Note Title 31-08-2012

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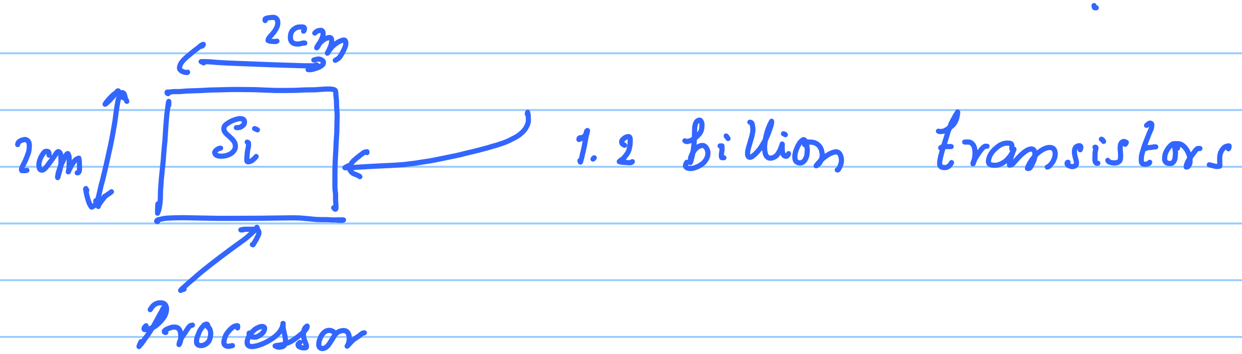
1) Computer A Computer B

4 GHz 3 GHz



Program

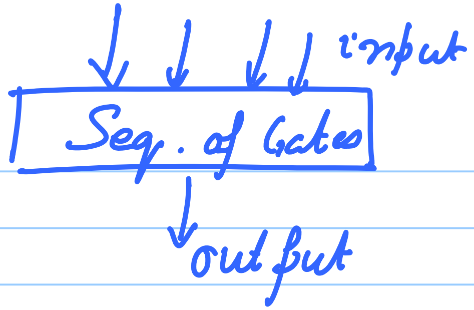
1) $a = b + c$ [2 ... 3.2 ns]
2) $d = e + a$
3) $f = d \times 2$
4) $g = \sqrt{f}$

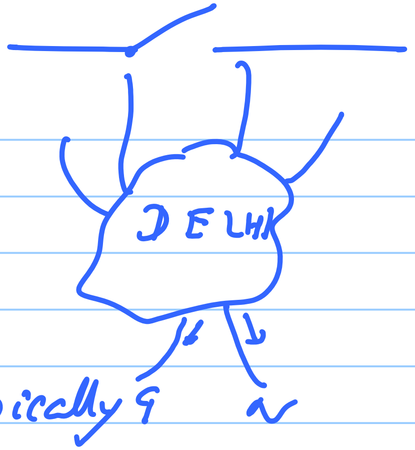
1) How does the hardware know when inst 1 has finished?

Simple Solution: Pass a token from inst 1 to inst. 2

Adder

→ How do you know when the adder has finished?

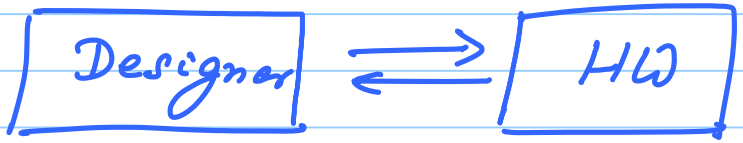




It is very hard to electronically detect that your computation is over.

Approach

Implicit constraint/contract



Designer

Ensure that the adder can complete its addition by (T) 2ns. (Irrespective of the inputs)

after time (T) the hardware will assume that the addition is over, It will use the result for other purposes.

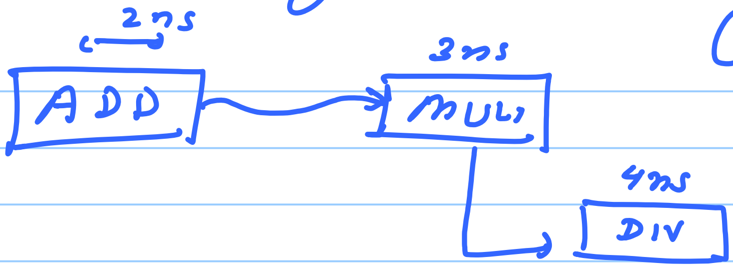
Designer' guarantee a certain time, T

Software simulation tools

(EDA tool) Electronic Design & Automation

GALS: Globally asynchronous locally synchronous

(Token passing)

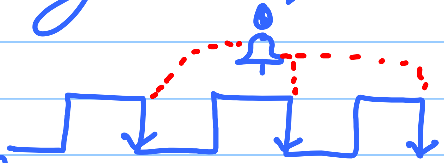


- Complicated
- You can have too many tokens
- managing tokens is difficult

Discretize Time

Globally synchronous

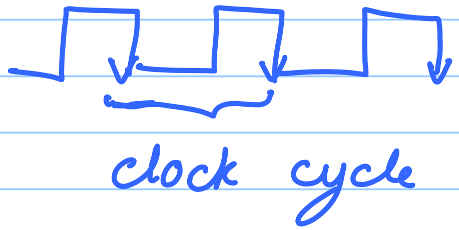
Clock



fed to every single circuit element

adder, multiplier, divider

Every circuit element synchronizes itself to the bell.



$$\text{clock frequency} = \frac{1}{\text{clock cycle}}$$

2 GHz : 500 ps

Represent time in clock cycles

Latency of adder: 1 cycle
multiplier: 2 cycle

+ eliminates the need for tokens

Google: Overclockers.

CPU Performance: $\frac{1}{(\text{seconds}/\text{program})}$

Measure the wall clock time.

$$\text{Perf} = \frac{1}{\#\text{ seconds}/\#\text{Programs}}$$

$$= \frac{\#\text{ Programs}}{\#\text{seconds}}$$

$$= \frac{\#\text{Programs}}{\#\text{ insts}} \times \underbrace{\frac{\#\text{ insts}}{\#\text{ cycles}}}_{(\text{IPC})} \times \underbrace{\frac{\#\text{ cycles}}{\#\text{ seconds}}}_{f\ (\text{frequency})}$$

[Instructions per cycle]

$$CPI = \frac{1}{IPC}$$

$$\left(Perf = \frac{IPC \times f}{\#\ insts\_per\_prog} \right)$$ Performance Equation

$f \rightarrow$ Hardware, Technology, Signal Integrity

Power & Temperature

$P \propto C V^2 f$ - - - - - ($V \propto f$)

freq.

supply voltage

capacitance

$P \propto f^3$ (Thumb rule)

- Double the freq.
- Power becomes 8 times

IPC → Architecture dependent parameters

$$\underset{\text{(dynamic)}}{\#\ \text{insts per program}} \rightarrow \left\{\begin{array}{c}\text{Programmer}\\ + \\ \text{compiler}\end{array}\right.$$

$$\left\{ \text{Perf} \propto \frac{\underset{(f)}{(\text{Technology})} \times \underset{\boxed{\text{IPC}}}{(\text{architecture})}}{\underset{(\text{compiler})}{\#\ \text{insts-per-prog}}} \right\}$$