

Oct -16

95% L1 SRAM (16KB, 1cyc)

66% L2 SRAM (64KB, 8cyc)

MEMORY DRAM (200cyc)
2GB

$f \rightarrow$ fraction of mem instr. = $\frac{1}{3}$

$$CPI = CPI_{ideal} + f [0.05 \times 8 + 0.05 \times \frac{1}{3} \times 200]$$

$$= CPI_{ideal} + \frac{1}{3} [0.4 + 3.33]$$

$$= [CPI_{ideal} + 1.24]$$

(i)

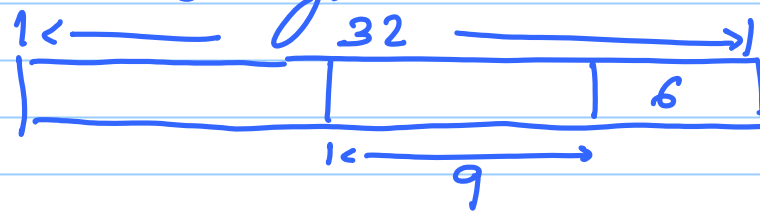
$$= \underline{2.24} \quad [w/ \text{Multilevel}]$$

$$CPI = 1 + \frac{1}{3} \times 200 = \underline{67.66}$$

IF ID EX MEM WB



Cache: Design.

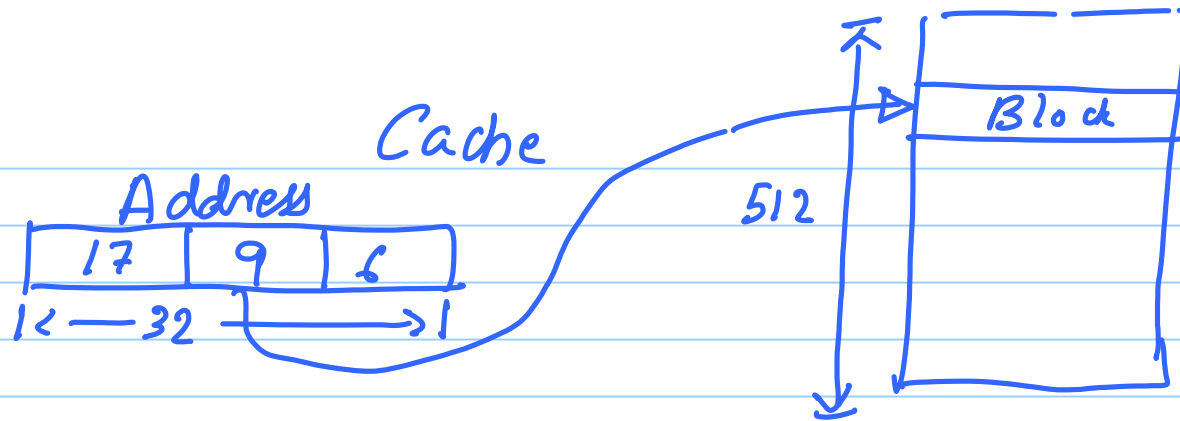


64 byte block.

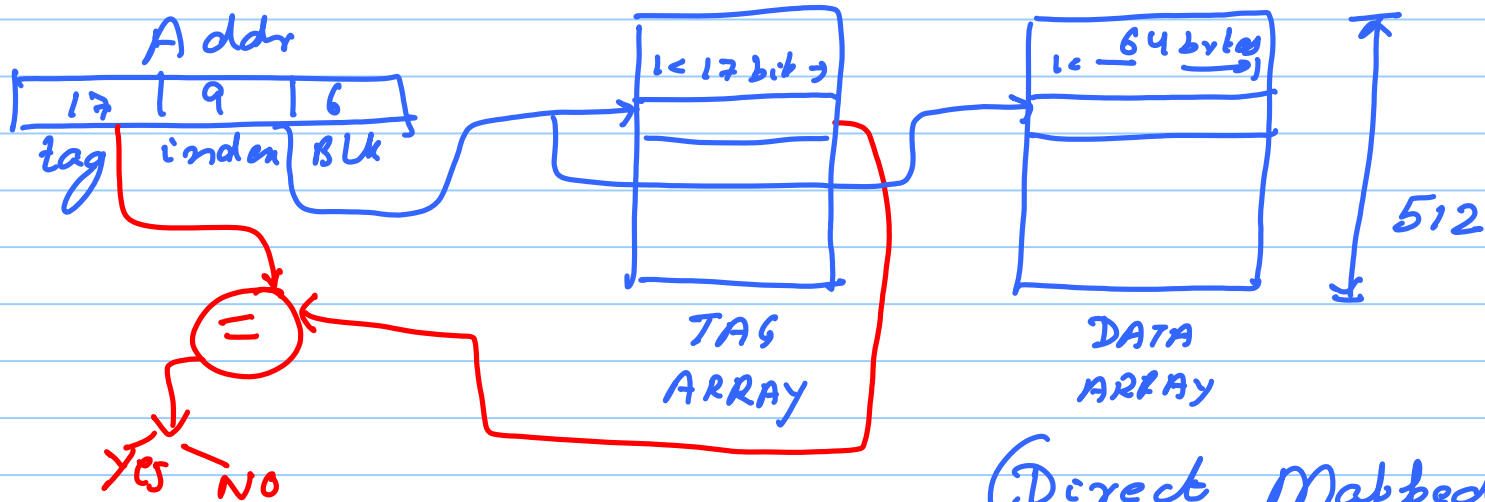
Cache size: $32 \text{ KB} = 2^{15}$

Block size: 64 bytes 2^6

of blocks: 2^9 (512)



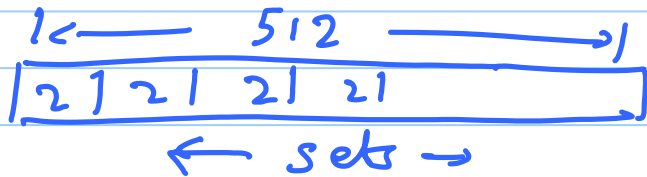
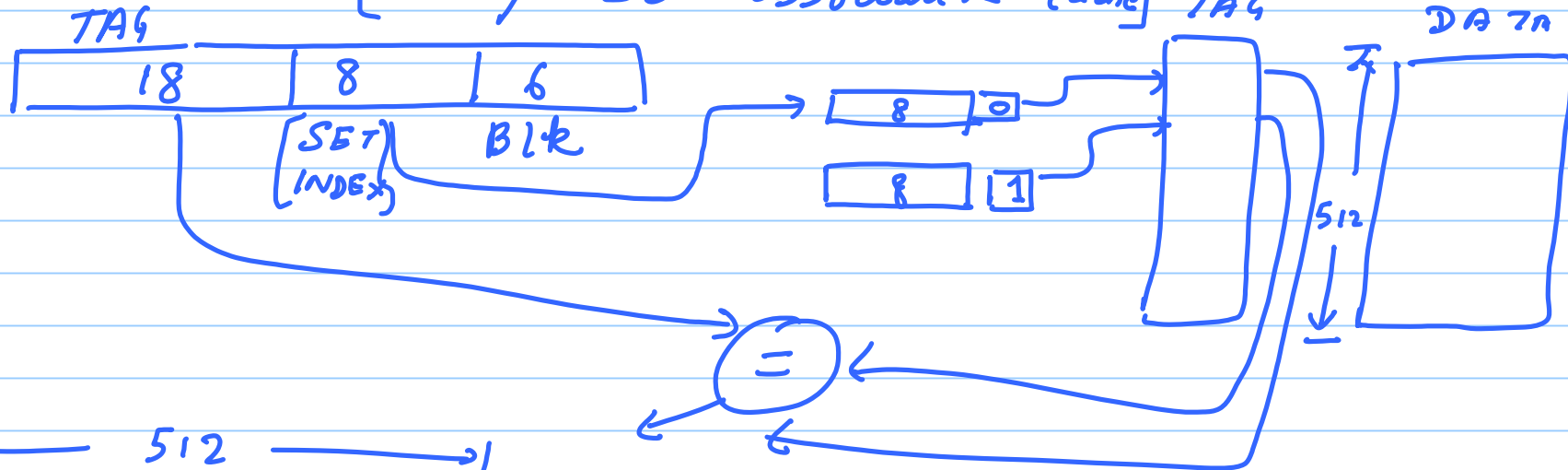
Structure of a cache



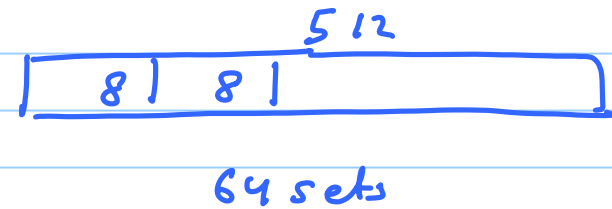
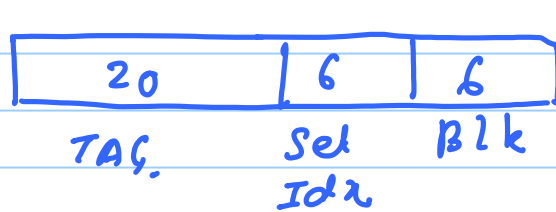
(Direct Mapped Cache)

1 0 0 0 0 0 → 32 $\overbrace{32\ 33\ 34\ 35}$
 1 0 0 0 0 1 → 33 $\overbrace{33\ 34\ 35\ 36}$

[2-way set associative cache] TAG



8-way set associative cache



Limiting Case: 512-way set assoc. cache
(Fully Assoc. Cache)

