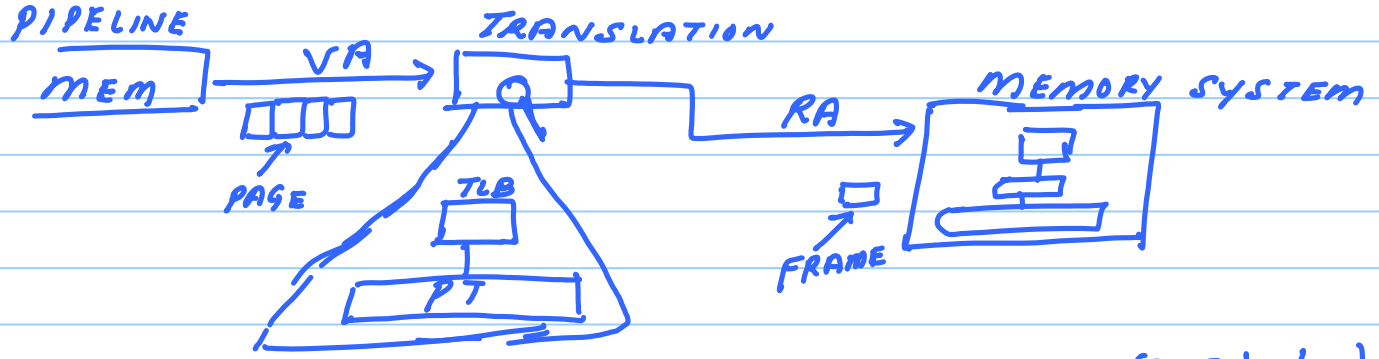
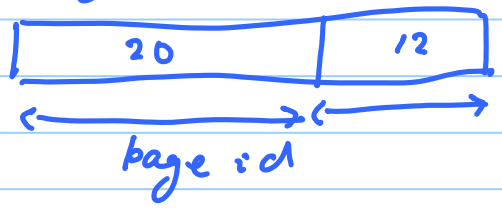
Nov 2nd Repair

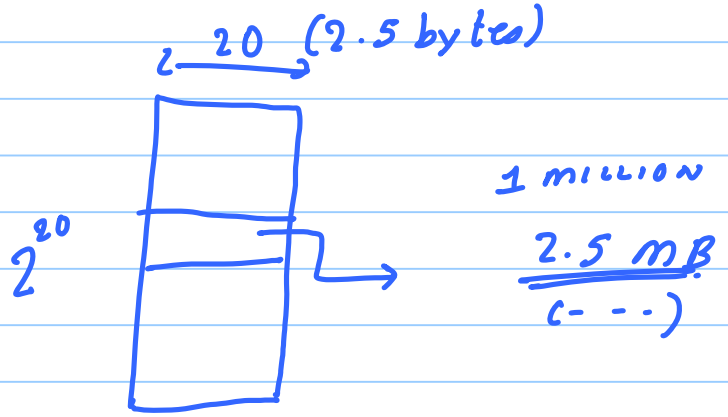
Note Title 02-11-2011

Multi-Level Page Tables.

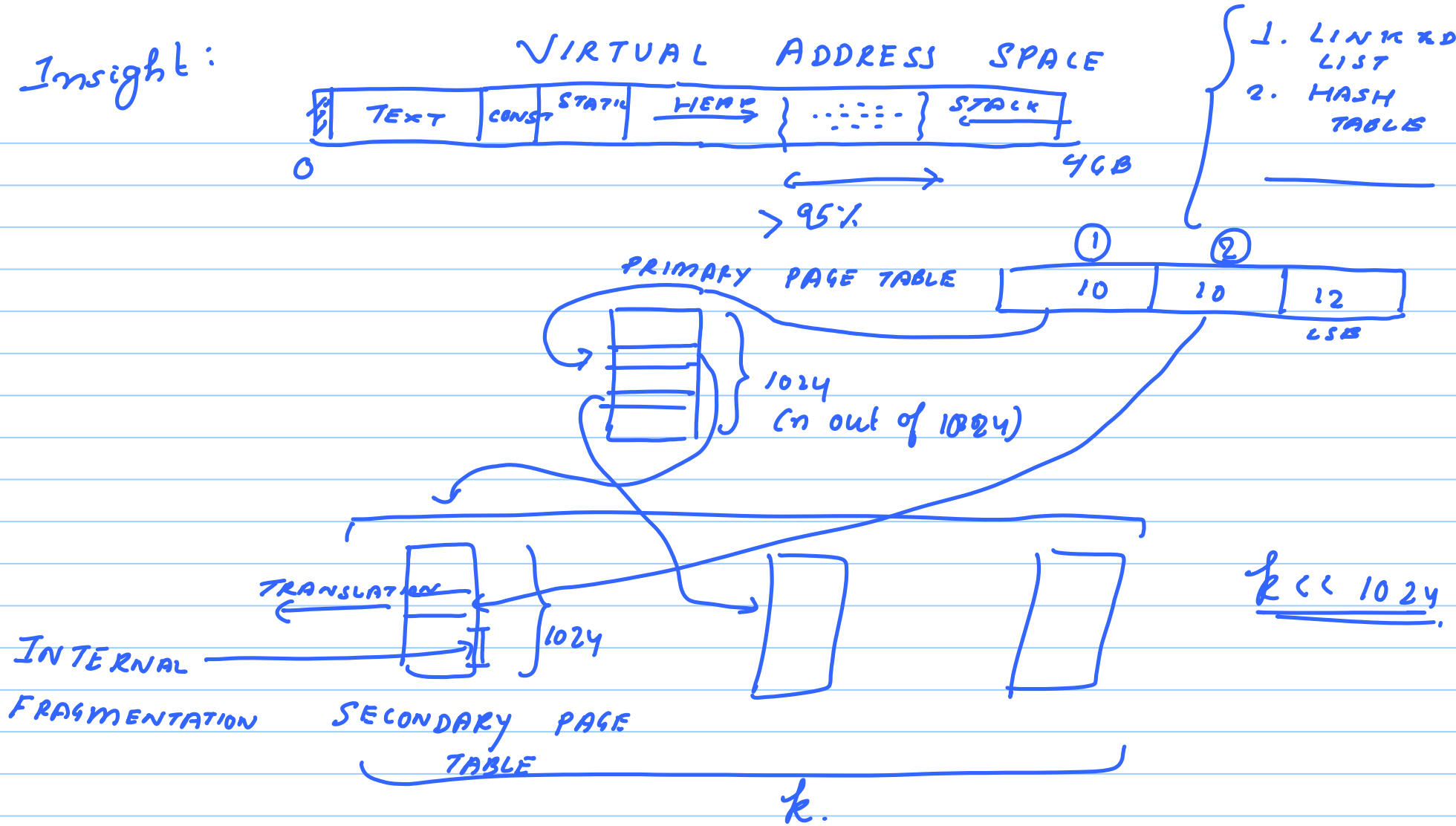


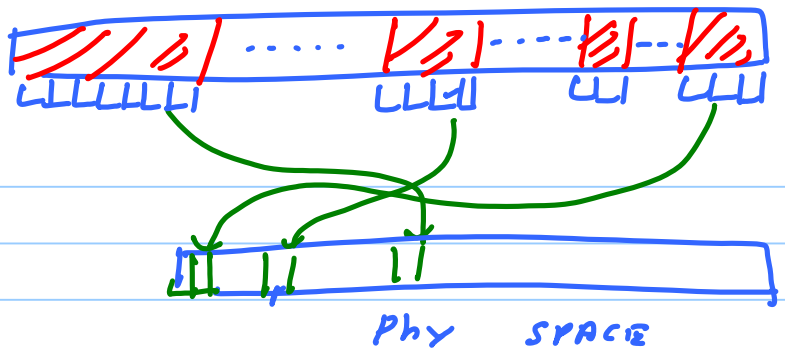
Single Level.





Insight:


VIRTUAL ADDRESS SPACE
TEXT
CONST
STATIC
HEAP
STACK
0
4GB
> 95%
1. LINKED LIST
2. HASH TABLES
PRIMARY PAGE TABLE
1
2
10
10
12
LSB
1024
(n out of 1024)
TRANSLATION
1024
INTERNAL FRAGMENTATION
SECONDARY PAGE TABLE
k
k << 1024



Alternative Organization:

Modify the single level page table → set associative cache.

400 MB / 4kB

1024

Cache Entries can be thrown out

Page Table Entries cannot be thrown out.

Multiprocessors.

COMPILER

BUNDLE

2 Instr. → PIPELINE

VLIW

Very Long Instruction Word

No dependences in a bundle

- Data
  - Register
    - RAW
    - WAR
    - WAW
  - Memory
- CONTROL

Register.

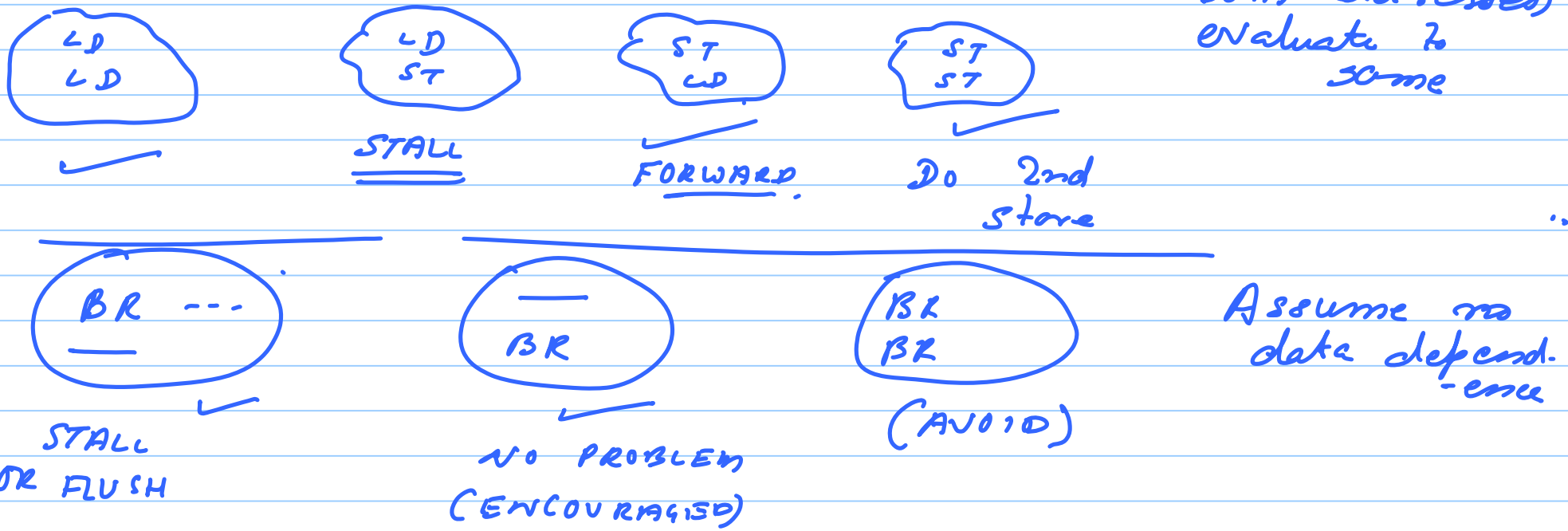
- RAW: $r_1 = r_2 + r_3$, $r_4 = 2 \times r_1$
- WAR: $r_1 = r_2 + r_3$, $r_2 = 6$
- WAW: $r_1 = 5$, $r_1 = 7$

IF	ID	Ex	M	WB
IF	ID	Ex	M	WB

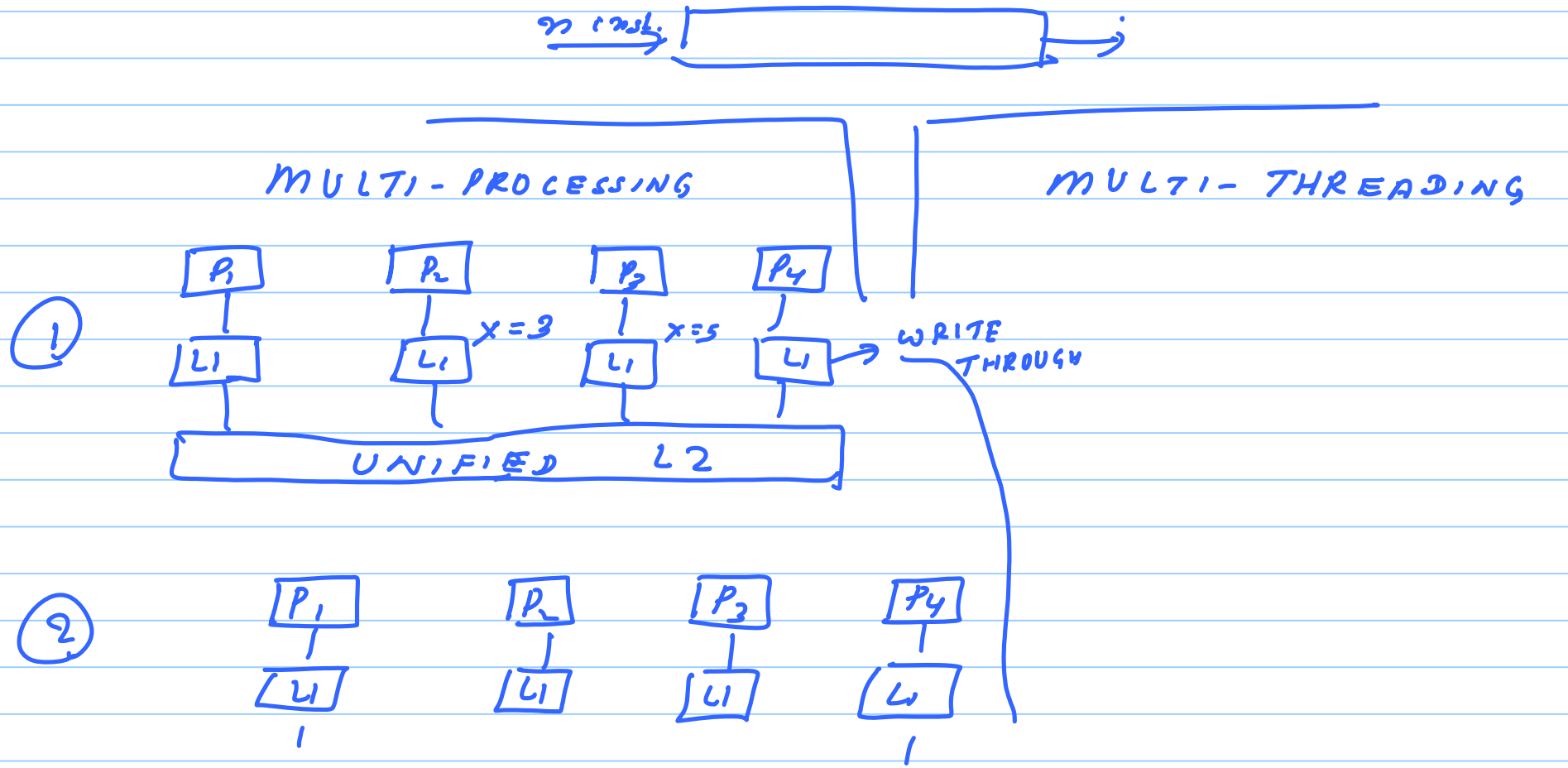
DON'T CREATE OR STALL

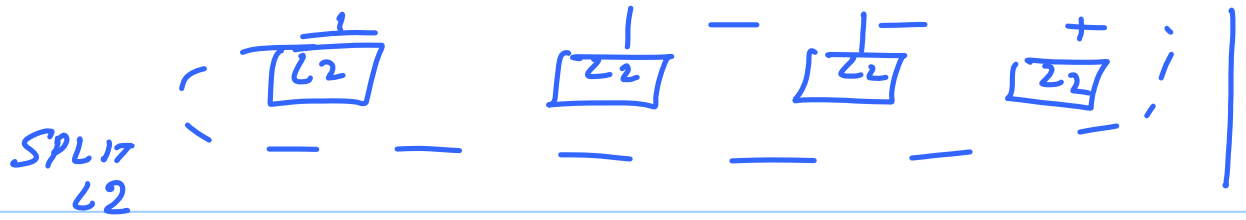
MEMORY.

NOT POSSIBLE TO PREDICT (At runtime both addresses) evaluate to same



FOUNDATIONS OF A MULTIPLE ISSUE PIPELINE





SW Definition

Process: Program with a separate address space

Threads: Group of programs with same address space

HW definition

Process: same as SW

Thread: Same address space & multiple threads run on the same processor.