

B. SHARAT CHANDRA VARMA

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- OBJECTIVE** Seeking a challenging position in the field of computer architecture and reconfigurable computing.
- RESEARCH INTERESTS** Reconfigurable Computing, FPGA, Hardware-Software Co-Design, Hardware Accelerators, Computer Architecture
- EDUCATION**
- | | |
|---|------------|
| PhD Candidate,
Amarnath Shashi Khosla School of IT
Indian Institute of Technology Delhi
New Delhi, India | Since 2008 |
| Master of Science
Major: VLSI-CAD
Manipal University
Karnataka, India | 2005-2007 |
| Bachelor of Engineering
Major: Electronics and Communication Engineering
Visvesvaraya Technological University
Karnataka, India | 1999-2003 |
- RESEARCH EXPERIENCE**
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| Research Intern
Symbiose Group
IRISA
Rennes, France
Worked on accelerating De Novo Genome Assembly using FPGAs.
www.irisa.fr | November 2011 - May 2012 (6 months) |
| Centre for High Performance Embedded Systems (CHIPES)
Nanyang Technological University, Singapore
Worked on implementing custom instruction in Leon soft-core processor.
www.chipes.ntu.edu.sg | December 2007 - May 2008 (6 months) |
| Alchemy group
INRIA Futurs, France
Study of SystemC internals.
www.inria.fr | August 2007 - October 2007 (3 months) |
- INDUSTRY EXPERIENCE**
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| Software Engineer
QuickLogic India Pvt Ltd., Bangalore, India.
Worked on EDA Tool development for QuickLogic FPGAs.
www.quicklogic.com | June 2006 - August 2007 (1 year 3 months) |
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Program Analyst Trainee May 2004 - October 2004 (6 months)

Cognizant Technology Solutions India Pvt. Ltd.,
Chennai, India.

Involved in the enhancement of software for IBM POS (point of Sale Machines) used by DFS(Duty Free Shopping) company. The coding was done in C-Basic.
www.cognizant.com

PUBLICATIONS

1. B. Sharat Chandra Varma, Kolin Paul, M. Balakrishnan, "Accelerating 3D-FFT Using Hard Embedded Blocks in FPGAs", 26th Proceedings of the International Conference on VLSI Design, Jan 2013, Pune, India
2. B. Sharat Chandra Varma, Kolin Paul, M. Balakrishnan, Dominique Lavenier, "FAssem : FPGA based Acceleration of De Novo Genome Assembly", FCCM 2013, April 2013, Seattle, USA
3. B. Sharat Chandra Varma, Kolin Paul, M. Balakrishnan, Dominique Lavenier, "Hardware Acceleration of De Novo Genome Assembly", Integration, the VLSI Journal, (Submitted Aug-2013)
4. B. Sharat Chandra Varma, Kolin Paul, M. Balakrishnan, "Accelerating Genome Assembly using Hard Embedded Blocks in FPGAs", International Conference on VLSI Design, (Accepted Jan-2014)
5. B. Sharat Chandra Varma, Kolin Paul, M. Balakrishnan, "High Level Design Space Exploration for accelerating De Novo Genome Assembly using FPGAs", International Symposium on Applied Reconfigurable Computing 2014 (submitted)

SKILL SET

HDL Languages: Verilog, VHDL, Impulse-C, SystemC

Simulation Tools: SPICE, Modelsim, Aldec (Active-HDL), **Layout Tool:** MAGIC

Synthesis Tools: Synopsys-Design Compiler (DC), QuickWorks, Precision RTL Synthesis, Xilinx ISE, **Assembly Languages:** 8085, 8086, **Programming:** C, CBASIC, C++

TEACHING ASSISTANT

CSL 101: Introduction to Computers and Programming

CSP 745: Digital Systems Design Laboratory

CSP 315: Embedded System Design

CSL 316: Digital Hardware Design

REFERENCES

Prof. M. Balakrishnan

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Dominique Lavenier

CNRS Research Director & GenScale team leader

IRISA / INRIA

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**PERSONAL
DETAILS**

Date of Birth: 30-09-1982

Languages Known: English, Telugu, Kannada and Hindi

Nationality: Indian