Smruti Ranjan Sarangi

CONTACT INFORMATION

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CURRENT POSITION

I am currently employed as an assistant professor in the Computer Science and Engineering Department at IIT Delhi. I teach courses and conduct research in computer architecture, operating systems, and parallel and distributed systems.

RESEARCH INTERESTS

Computer Architecture(Primary Interest): Reliability, Hardware support for operating systems, Optical networking, Temperature aware processors.
Parallel Algorithms: Non-blocking data structures, Wait-free slot schedulers
Operating Systems: Jitter free operating systems, HW/SW codesign of operating systems
Total Research Contribution: 14 Journal papers, 41 Conference papers, 5 US Patents, 2 best paper awards + 1 nomination, 1.3 crores of research funding (as PI)

EDUCATION

University of Illinois at Urbana-Champaign, IL(UIUC)

Ph.D., Computer Science, May 2007 (GPA 3.95/4.00)
Thesis Title: Techniques to Mitigate the Effects of Congenital Faults in Processors
Advisor: Josep Torrellas

University of Illinois at Urbana Champaign, IL(UIUC)

M.S., Computer Science, Dec, 2004 (GPA 3.95/4.00)

Indian Institute of Technology, Kharagpur, India

B.Tech, Computer Science, May 2002 (GPA 9.33/10.00)

EMPLOYMENT

Computer Science and Engg. Deptt., IIT Delhi

Associate Professor (Jan 2017 till date)

Computer Science and Engg. Deptt., IIT Delhi

Assistant Professor (Jan 2011 till Jan 2017)

IBM Research Labs, Bangalore

Research Staff Member (April 2009 till Jan 2011)

India Systems and Technology Labs, IBM, Bangalore

Advisory Research Engineer (Nov 2007 till March 2009)

Synopsys Research, Bangalore

Researcher (March 2007 to Nov 2007)

Books

[**Textbook**] Computer Organisation and Architecture by Smruti R. Sarangi, 688 pages, McGrawHill, 2014.

[**Reference Book**] Techniques to Mitigate the Effects of Congenital Faults in Processors by Smruti R. Sarangi and Josep Torrellas 160 pages, ISBN: 978-3-639-04637-3, VDM Verlag, 2008. (based on Ph.D thesis)

Honors and Awards

Visvesvaraya Young Faculty Fellowship, 2014-15, by the Ministry of IT and Telecommunications, Government of India.

Best paper award received at the Security and Privacy Symposium for the paper, "Ethical Hacking of License Managers." (2015)

Teaching excellence award, best undergraduate teacher in the large class category, 2014.

Nucleus group young faculty award (IIT Delhi), 2011.

IBM Chairman's Equity Award (Top 1% in every unit), Nov 17, 2008.

Recognized as IBM Top Talent(Top 10% in every unit) since June 2008.

"Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware", selected in IEEE Micro Top picks. (top 13 papers in computer architecture in 2006)

"Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware", **Best Paper Award, MICRO 2006**

"Energy-Efficient Thread-Level Speculation on a CMP" selected in IEEE Micro Top picks. (top 13 papers in computer architecture in 2005)

David J. Kuck, Best MS thesis award in the department of computer science, UIUC in 2004.

Ranked 170/150,000 in the IIT Joint Entrance Examination, India, 1998.

Ranked 50/30,000 in the Indian National Physics Olympiad, 1998.

Ranked 65/25,000 in the Indian Maths Olympiad, 1997.

National Talent Search Exam scholarship, India, 1996. ranked 35/40,000.

Professional Service

Member of the program committees of HiPC, IPDPS, ICDCIT	**2013-15**
Student Symposium Chair: HiPC	**Dec. 2010**
Program Committee Member: HiPC	**Dec. 2010**

Workshop Chair : Cloud Computing held along with HIPC	**Dec. 2009**
Workshop/Tutorials Chair for PPoPP	**Dec. 2009**
Registration chair for HPCA	**Dec. 2009**
Student Research Co-ordinator for HiPC	**Dec. 2009**
Program Committee member for NISS, NCM, ICCIT	**2009**

Reviewed papers for HPCA, MICRO, ISCA, OSDI, ASPLOS, PPopp, PLDI, HiPC, CGO, PODC, DSN, HiPC, IPDPS, DAC, ACM TACO, IEEE TPDS.

TEACHING EXPERIENCE

Courses taught at IIT Delhi (600+ students): Advanced Distributed Systems, Principles of Multiprocessor Systems, Computer Architecture, Fault Tolerant Systems, Architecture of High Performance Computers

Teaching Outreach activity:

1. Conducted workshops for school children preparing for the international informatics olympiad at IIIT Delhi. (2014 and 2015)
2. Taught the computer architecture course at IIT Ropar for 2 years (via video) (2011 and 2012).
3. Taught a remote course for students at the Addis Abbaba university, Ethiopia. (2011)

Publications

International Journal Papers

1. FluidCheck: A Redundant Threading based Approach for Reliable Execution in Manycore Processors, Rajshekar Kalayappan, and Smruti R. Sarangi. ACM Transactions on Architecture and Code Optimization (TACO). Volume 12 Issue 4, January 2016. Also presented at the European Network on High Performance and Embedded Architecture and Compilation Conference (HiPEAC) 2016, Prague.
2. Active Microring Based Tunable Optical Power Splitters, Eldhose Peter, Arun Thomas, Anuj Dhawan, Smruti R. Sarangi. Optics Communications, Volume 359, Pages 311 – 315, 2016
3. Area-aware Cache Update Trackers for Post-silicon Validation, Sandeep Chandran, Smruti R. Sarangi, Preeti Panda, IEEE Transactions on VLSI Systems (accepted in 2015).
4. Lock-free and Wait-free Slot Scheduling Algorithms by Pooja Aggarwal and Smruti R. Sarangi, IEEE Transactions on Parallel and Distributed Systems, Volume 27, Issue 5, Pages: 1387-1400, 2016
5. FP-NUCA: A Fast NOC Layer for Implementing Large NUCA Caches, Anuj Arora, Mayur Harne, Hameedah Sultan, Akriti Bagaria, Smruti R. Sarangi. IEEE Transactions on Parallel and Distributed Systems. Volume: 26, Issue: 9 Pages: 2465 - 2478, 2015.
6. Processor Power Estimation Techniques: A Survey, Hameedah Sultan, Gayathri Ananthanarayanan, and Smruti R. Sarangi. International Journal of High Performance Systems Architecture. Volume 5 Issue 2, May 2014, Pages 93-114
7. Architectural Support for Handling Jitter in Shared Memory based Parallel Applications by Sandeep Chandra, Prathmesh Kallurkar, Parul Gupta, Smruti R. Sarangi,

IEEE Transactions on Parallel and Distributed Systems. Volume 25, Issue 5, Pages: 1166-1176, May 2014

8. Amdahl's Law in the Era of Process Variation by Gayathri Ananthanarayanan, Geetika Malhotra, M. Balakrishnan, and Smruti R. Sarangi. International Journal of High Performance Systems Architecture (IJHPSA). 2013, Vol 4, No. 4. pp 218-230.
9. A Survey of Checker Architectures by Rajshekar Kalayappan and Smruti R. Sarangi, ACM Computing Surveys, Volume 45, Issue 4, Number 48, 2013.
10. IT Infrastructure for Providing Energy-as-a-Service to Electric Vehicles by Smruti R. Sarangi, Partha Dutta, and Komal Jalan in IEEE Transactions on Smart Grids. Vol. 3, Issue 2, pages 594-604, 2012.
11. VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects by Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, IEEE Transactions on Semiconductor Manufacturing (IEEE TSM), February 2008. Volume 21, Issue 1, pp 3–13
12. Patching Processor Design Errors with Programmable Hardware, Smruti R. Sarangi, Satish Naraya- naswamy, Bruce Carneal, Abhishek Tiwari, Brad Calder, Josep Torrellas. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture, Jan. 2007, Volume 27, Issue 1, pages 12–25.
13. Energy-Efficient Thread-Level Speculation on a CMP by Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti R. Sarangi, James Tuck and Josep Torrellas. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture, Jan. 2006, Volume 26, Issue 1, pages 80–91
14. A Scalable Efficient and General Monte Carlo Scheme for Generating Synthetic Web Request Streams by Smruti R. Sarangi, P.N.Sireesh and S.P.Pal. International Journal of Computer Systems Science and Engineering, Vol. 18, pp, 121-128, May 2003.

International Conference Papers

1. Leakage Power Aware Task Assignment Algorithms for Multicore Platforms, Gayathri Ananthanarayanan, Smruti R. Sarangi, M. Balakrishnan, International Annual Symposium on VLSI (ISVLSI), Pittsburgh, USA (accepted)
2. SecCheck: A Trustworthy System with Untrusted Components, Rajshekar Kalayappan, Smruti R. Sarangi, International Annual Symposium on VLSI (ISVLSI), Pittsburgh, USA (accepted)
3. Noise Aware Scheduling in Data Centers, Hameedah Sultan, Arpit Katiyar, Smruti R. Sarangi. International Conference on Supercomputing (ICS), 2016. Istanbul (accepted)
4. OptiShare: A Dynamic Channel Sharing Scheme for Power Efficient On-chip Optical Architectures, Eldhose Peter, Smruti R. Sarangi, OPTICS workshop, along with Design Automation and Test in Europe (DATE) 2016, Dresden, Germany
5. A Wait-Free Stack, Seep Goel, Pooja Aggarwal, Smruti R. Sarangi, International Conference on Distributed Computing and Internet Technology (ICDCIT), Bhubaneshwar, 2016

6. A Generic Implementation of Barriers using Optical Interconnects, Sandeep Chandran, Eldhose Peter, Preeti R. Panda, Smruti R. Sarangi, VLSI Design, Kolkata, 2016
7. Extending Trace History Through Tapered Summaries in Post-silicon Validation, Sandeep Chandran, Preeti Ranjan Panda, Smruti R. Sarangi, Deepak Chauhan, Sharad Kumar, Asia and South Pacific Design Automation Conference (ASPDAC), Macao, 2016. **(Nominated for the Best Paper Award)**
8. ColdBus: A Near-Optimal Power Efficient Optical Bus, Eldhose Peter, Arun Thomas, Anuj Dhawan, Smruti R. Sarangi, HiPC (High Performance Computing), Bangalore, 2015.
9. Tejas: A Java based Versatile Micro-architectural Simulator, Smruti R. Sarangi, Rajshekar Kalayappan, Prathmesh Kallurkar, Seep Goel, Eldhose Peter. PATMOS, Salvador Brazil, 2015.
10. SecX: A Framework for Collecting Runtime Statistics for SoCs with Multiple Accelerators, Rajshekar Kalayappan and Smruti R. Sarangi, ISVLSI, Montpeller, France, 2015
11. Ethical Hacking of License Managers, Karishma Agarwal, Prathmesh Kallurkar, Siva Krishna Aleti, Smruti R. Sarangi. Security and Privacy Symposium, IIIT Delhi, 2015 **(Best Paper Award)**.
12. Optimal Power Efficient Photonic SWMR Buses, Eldhose Peter, Smruti R. Sarangi, 2nd Workshop on Silicon Photonics, along with the HiPEAC Conference, Amsterdam, 2015.
13. RADIR: Lock-free and Wait-free Bandwidth Allocation Models for Solid State Drives, Pooja Aggarwal, Giridhar Yasa, Smruti R. Sarangi, HiPC, Goa, 2014.
14. Optical Overlay NUCA: A High Speed Substrate for Shared L2 Caches, Eldhose Peter, Anuj Arora, Akriti Bagaria, Smruti R. Sarangi, HiPC, Goa, 2014.
15. Trikon: A Hypervisor Aware Manycore Processor, Rohan Bhalla, Prathmesh Kallurkar, Nitin Gupta, Smruti R. Sarangi, HiPC, Goa, 2014.
16. GPUTejas: A Parallel Simulator for GPU Architectures, Geetika Malhotra, Seep Goel, Smruti R. Sarangi, HiPC, Goa, 2014.
17. ParTejas: A Parallel Simulator for Multicore Processors, Geetika Malhotra, Pooja Aggarwal, Abhishek Sagar, Smruti R. Sarangi. ISPASS, Monterey, CA, US, 2014.
18. Software Transactional Memory Friendly Slot Schedulers by Pooja Aggarwal, and Smruti R. Sarangi, ICDCIT, Bhubaneswar, 2014.
19. OptiKit: An Open Source Kit for Simulation of On-Chip Optical Components by Eldhose Peter, and Smruti R. Sarangi. VLSI Design (Poster), Mumbai, 2014.
20. LightSim : A Leakage Aware Ultrafast Temperature Simulator by Smruti R. Sarangi, Gayathri Ananthanarayanan, and M. Balakrishnan, ASP-DAC, Singapore, 2014.
21. A Case Study of a First-of-Its-Kind Remote Course among Premier Institutions in India by Smruti R. Sarangi, International Conference on E-Learning and E-Technologies in Education, (ICEEE), Lodz, Poland, 2013.
22. emuArm: A Tool for Teaching the ARM Assembly Language by Geetika Malhotra, Namita Atri, Smruti R. Sarangi, International Conference on E-Learning and E-Technologies in Education, (ICEEE), Lodz, Poland, 2013.

23. Space Sensitive Cache Dumping for Post Silicon Validation by Sandeep Chandran, Smruti R. Sarangi, Preeti Ranjan Panda, Design Automation and Test in Europe (DATE), Grenoble, France, 2013.
24. Lock-free and Wait-free Slot Scheduling Algorithms by Pooja Aggarwal, Smruti R. Sarangi, International Parallel and Distributed Processing Symposium (IPDPS), Boston, USA, 2013.
25. Efficient on-line algorithms for maintaining k-cover of a sparse bit-string by Amit Kumar, Preeti Panda, Smruti R. Sarangi, Foundations of Software Technology and Theoretical Computer Science (FSTTCS), Hyderabad, India, 2012.
26. UsiFe: An User Space Filesystem with Support for Intra File Encryption by Rohan Sharma, Prathmesh Kallurkar, Saurabh Kumar, and Smruti R. Sarangi, International Conference on Software and Computing Technology (ICSCT), Singapore, 2011.
27. Virtualized Base Station Pool : Towards a Wireless Network Cloud for Radio Access Networks by Zhenbo Zhu, Qing Wang, Yonghua Lin, Parul Gupta, Smruti R. Sarangi Shivkumar Kalyanaraman, Hubertus Franke. ACM Computing Frontiers, Italy, 2011.
28. DUST: A Generalized Notion of Similarity between Uncertain Time Series by Smruti R. Sarangi, and Karin Murthy.Knowledge Discovery and Data Mining(KDD), Washington D.C., USA, 2010.
29. Theoretical Framework for Eliminating Redundancy in Workflows by Dhrubajyoti Saha, Abhishek Samanta, and Smruti R. Sarangi. IEEE International Conference on Service Computing (SCC), Bangalore, September 2009.
30. High Performance SWR Base Station and Wireless Network Cloud over General Multicore IT Platforms by Yonghua Lin, Qing Wang, Zhenbo Zhu, Jianwen Chen, Lin Chen, Rong Yan, Wei Xie, Kuan Feng, Parul Gupta, Smruti R. Sarangi (demo paper) in MobiCom, Beijing, 2009.
31. EVAL: Utilizing Processors with Variation-Induced Timing Errors by Smruti Sarangi, Brian Greskamp, Abhishek Tiwari, and Josep Torrellas. 41st International Symposium on Microarchitecture (MICRO), Lake Como, Italy, November 2008.
32. VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects by Radu Teodorescu, Brian Greskamp, Jun Nakano, Smruti Sarangi, Abhishek Tiwari, and Josep Torrellas (UIUC). 2nd Workshop on Architectural Support for Gigascale Integration (ASGI) (along with ISCA 2007), San Diego, USA, June 2007.
33. ReCycle: Pipeline Adaptation to Tolerate Process Variation by Abhishek Tiwari, Smruti Sarangi, and Josep Torrellas, 34th Annual International Symposium on Computer Architecture (ISCA), San Diego, USA, June 2007.
34. Threshold Voltage Variation Effects on Aging-Related Hard Failure Rates by Brian Greskamp, Smruti Sarangi, and Josep Torrellas. International Symposium on Circuits and Systems (ISCAS), Special Session: Circuit Design in the Presence of Device Variability, Taipei, May 2007.
35. A Model for Timing Errors in Processors with Parameter Variation by Smruti Sarangi, Brian Greskamp, and Josep Torrellas. 8th International Symposium on Quality Electronic Design (ISQED), March 2007.
36. Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware by Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas.

39th International Symposium on Microarchitecture (MICRO), Dec. 2006. **(Best Paper Award)**

37. Designing Hardware that Supports Cycle-Accurate Deterministic Replay by Brian Greskamp, Smruti R. Sarangi and Josep Torrellas. Workshop on Complexity Effective Design(WCED) (along with ISCA 2006).
38. Rapid Prototyping in Architecture Research using Existing Hardware Mechanisms by Smruti R. Sarangi, Brian Greskamp and Josep Torrellas. Workshop on Architectural Research Prototyping(WARP) (along with ISCA 2006).
39. Cycle-Accurate Deterministic Replay for Processor Debugging by Smruti R. Sarangi Brian Greskamp and Josep Torrellas. Dependable Systems and Networks (DSN) 2006.
40. ReSlice: Selective Re-Execution of Long-Retired Misspeculated Instructions Using Forward Slicing by Smruti R. Sarangi, Wei Liu, Josep Torrellas, and Yuanyuan Zhou. 38th International Symposium on Microarchitecture (MICRO), November 2005.
41. Thread-Level Speculation on a CMP Can Be Energy Efficient by Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. 2005 ACM International Conference on Supercomputing (ICS), June 2005.

Patents Filed

1. Systems and methods for exploring and utilizing solutions to cyber-physical issues in a sandbox, Ullas Nambiar, Smruti R. Sarangi, Biplav Srivastava, Vivek Tyagi, IBM Corp. US PTO Number: US 13/088,915
2. Distributed symbol table with intelligent lookup scheme, Sikta Pany, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/717,601
3. Optimizing Workflow Engines, Dhrubajyoti Saha, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/726,798
4. Accelerating Generic Loop Iterators Using Speculative Execution, Ganesh Bikshandi, Dibyendu Das, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/938,312
5. Generalized notion of similarities between uncertain time series, Karin Murthy, Smruti R. Sarangi, IBM Corp. US PTO Number: US 12/833,055

Research Projects

Smruti Ranjan Sarangi				
S. No.	Title	Cost	Duration	Agency
as PI				
1	Process Verification aware computer architecture	1 lakh	2011-12	IIT Delhi
2	Temperature Aware Placement in Large Multicore Processors, Planning	10 lakhs	2011-13	IIT Delhi
3	BhartiSim: An Advanced Micro-architectural Simulator	61 lakhs	2012-15	Ministry of IT
4	Lock Free Algorithms for Scheduling in Storage Systems	13 lakhs	2013-14	Netapp India Pvt. Ltd.
5	Design of Energy Efficient Optical Networks in Multicore Processors	33 lakhs	2014-17	Department of Science and Technology
6	Characterization of Operating Systems for System Intensive Workloads	12.5 lakhs	2015-17	Netapp India Pvt. Ltd.
as co-PI				
7	Characterization of Multi-core Processors for Power-Estimation at System-Level	15.5 lakhs	2011-13	DST
8	Structured Sharing of Networks and Computer Resources in a Community of Devices	200k USD	2013-16	Intel, USA
9	Advanced Debug Architecture and Methodology for Hetrogeneous Multicore Platforms	32 lakhs	2014-17	Semiconductor Research Corporation