Mapping C/C++ Concurrency to Processors
### Recap: C/C++ Mapping to x86

<table>
<thead>
<tr>
<th>C11</th>
<th>x86</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{na}</td>
<td>mov(R)</td>
</tr>
<tr>
<td>R_{rlx}</td>
<td>mov(R)</td>
</tr>
<tr>
<td>R_{acq}</td>
<td>mov(R)</td>
</tr>
<tr>
<td>R_{sc}</td>
<td>mov(R)</td>
</tr>
<tr>
<td>W_{na}</td>
<td>mov(W)</td>
</tr>
<tr>
<td>W_{rlx}</td>
<td>mov(W)</td>
</tr>
<tr>
<td>W_{rel}</td>
<td>mov(W)</td>
</tr>
<tr>
<td>W_{sc}</td>
<td>mov(W); mfence</td>
</tr>
<tr>
<td>U_{o}</td>
<td>lock cmpxchg</td>
</tr>
<tr>
<td>F_{sc}</td>
<td>skip</td>
</tr>
<tr>
<td>F_{&quot;sc}</td>
<td>mfence</td>
</tr>
</tbody>
</table>
Alternative Proof for x86 Mappings

$x_86 = \text{WR reordering} + \text{RAW elimination} + \text{interleaving}$

[Lahav:FM:2016].

C11 model supports WR reordering and RAW elimination.
### Mapping to PowerPC

<table>
<thead>
<tr>
<th>C11</th>
<th>PowerPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&lt;sub&gt;na&lt;/sub&gt;</td>
<td>R</td>
</tr>
<tr>
<td>R&lt;sub&gt;rlx&lt;/sub&gt;</td>
<td>R</td>
</tr>
<tr>
<td>R&lt;sub&gt;acq&lt;/sub&gt;</td>
<td>R; lwsync</td>
</tr>
<tr>
<td>W&lt;sub&gt;na&lt;/sub&gt;</td>
<td>W</td>
</tr>
<tr>
<td>W&lt;sub&gt;rlx&lt;/sub&gt;</td>
<td>W</td>
</tr>
<tr>
<td>W&lt;sub&gt;rel&lt;/sub&gt;</td>
<td>lwsync; W</td>
</tr>
<tr>
<td>F&lt;sub&gt;rel&lt;/sub&gt;</td>
<td>lwsync</td>
</tr>
<tr>
<td>F&lt;sub&gt;acq&lt;/sub&gt;</td>
<td>lwsync</td>
</tr>
</tbody>
</table>
Example

\[ X_{na} = 1; \]
\[ Y_{rel} = 1; \]
\[ a = Y_{acq}; \quad // \ 1 \]
\[ \text{if}(a == 1) \]
\[ b = X_{na}; \quad // \neq 0 \]

\[ X = 1; \]
\[ \text{lwsync}; \]
\[ a = Y; \quad // \ 1 \]
\[ \text{lwsync}; \]
\[ \text{if}(a == 1) \]
\[ b = X; \quad // \neq 0 \]

\[
[b = X; \quad // \ 0] \text{ would create (fr; prop) cycle.}
\]
Before Proving Correctness

\begin{align*}
W_{\text{rel}} & \sim F_{\text{rel}}; W_{\text{rlx}} \\
R_{\text{acq}} & \sim R_{\text{rlx}}; F_{\text{acq}}
\end{align*}

We prove $P_{C11} \leftrightarrow P_{Pow}$ in two steps:

$P_{C11} \leftrightarrow P_{C11}^F \leftrightarrow P_{Pow}$

$P_{C11} \leftrightarrow P_{C11}^F$ holds.

It suffices to show $P_{C11}^F \leftrightarrow P_{Pow}$ is correct.
Consider $X'$ execution in PowerPC and the corresponding C11 execution is $X$.

(irrHB)
Assume a $X$.hb cycle.
It implies a $(X$.po $\cup X$.swe$)^+$ cycle.
It implies
$X$.po; $[X$.F$_{rel}]$; $X$.po; $[X$.W$]$; $X$.rfe; $X$.hb$^?$; $X$.po; $[X$.F$_{acq}]$; $X$.hb$^?$
cycle.
Now $X$.po; $[X$.F$_{rel}]$; $X$.po; $[X$.W$]$; $X$.rfe in C11 implies
$X'$.fence; $[X'$.W$]$; $X'$.rfe in PowerPC.
It implies $X'$.hb in PowerPC.
Similarly
\[ X.p\; \exists \; [X.F_{\text{acq}}]; \; X.hb? \]
\[ \implies \]
\[ X.p\; \exists \; [X.F_{\text{acq}}]; \; X.p\; \exists \; [X.W]; \; X.rfe?; \; X.hb? \]
Now \[ X.p\; \exists \; [X.F_{\text{acq}}]; \; X.p\; \exists \; [X.W]; \; X.rfe? \]
\[ \implies \]
\[ X'.\text{fence}; \; [X'.W]; \; X'.rfe? \]
\[ \implies X'.hb \]
Thus \[ X.hb \implies X'.hb \] and we know \[ X'.hb \] is acyclic.
Hence a contradiction and \[ X.hb \] is acyclic and satisfies (irrHB).

Similarly prove the coherence axioms.
(CohHBRF)
Assume a $X_{rf}; X_{hb}$ cycle.
It implies a $X_{rf}; (X_{po} \cup X_{swe})^+$ cycle.
Two possibilities:
(1) $X_{rf}; X_{po_x}$ cycle.
It implies a $X'_rf; X_{po_x}$ cycle which is a contradiction.
(2) $X_{rf}; (X_{hb} \setminus X_{po})$ cycle.
It implies $X'_rfe; X'_hb$ i.e. a $X'_hb$ cycle which is a contradiction.
Therefore $X$ satisfies (CohHBRF).
Exercise. Prove the rest of the coherence axioms and atomicity.

Hint. For \texttt{mo} and \texttt{fr} related coherence axioms in C11 use prop axioms in PowerPC.

Referred Link:
https://www.cl.cam.ac.uk/~pes20/cpp/cpp0xmappings.html