ARMv8 Architecture
Some Observations from ARMv7

Non-intuitive behaviors.

\[ R(X, 2) \]
\[ W(Y, 1) \]
\[ W(X, 1) \]
\[ R(Y, 1) \]
\[ W(X, 2) \]
Some Observations from ARMv7

Non-multicopy atomic behavior

\[ W(X, 1) \xrightarrow{\text{rfe}} R(X, 1) \]
\[ R(Y, 0) \xrightarrow{\text{addr}} R(Y, 1) \]
\[ R(X, 0) \xleftarrow{\text{addr}} R(X, 1) \]

\[ W(Y, 1) \xrightarrow{\text{rfe}} R(Y, 1) \]
\[ R(X, 0) \xleftarrow{\text{addr}} R(X, 1) \]
Major Changes

Simplified ARM model.
- Removes non-multicopy atomicity.

Introduce stronger memory accesses and weaker fences

Additional memory accesses:
- Release-store: STLR (L)
- Acquire-load: LDAR (L)

Additional Fences:
- Load DMB (dmbld)
- Store DMB (dmbst)
Rules of New Primitives

STLR and LDAR constrains data access movement

- Accesses before an STLR are 'barrier-ordered-before’ the STLR
- LDAR is 'barrier-ordered-before’ following accesses
- STLR is 'barrier-ordered-before’ following LDAR

Fence Rules:

- `dmbfull` is a full fence
- `dmbld` orders a load (R) with a following load (R) or store (W)
- `dmbst` orders a store (W) with a following store (W)
ARMv8 Relations

Coherence-after: \( ca = fr \cup mo \)

Observed-by: \( obs = rfe \cup fre \cup moe \)

Dependency-ordered-before:

\[
dob = addr \cup data \\
\cup ctrl; [W] \\
\cup (ctrl \cup (addr; po)); [isb]; po; [R] \\
\cup addr; po; [W] \\
\cup (ctrl \cup data); moi \\
\cup (addr \cup data); rfi
\]
Atomic-ordered-before: \( aob = rmw \cup [\text{range}(rmw)]; rfi; [A] \)

Barrier-ordered-before:

\[
bob = po; [\text{dmbfull}]; po \\
\quad \cup [L]; po; [A] \\
\quad \cup [R]; po; [\text{dmbld}]; po \\
\quad \cup [A]; po \\
\quad \cup [W]; po; [\text{dmbst}]; po; [W] \\
\quad \cup po; [L] \\
\quad \cup po; [L]; coi
\]

Ordered-before: \( ob = (obs \cup dob \cup aob \cup bob)^+ \)
ARMv8 Axioms

\((po \cup fr \cup mo \cup rf)\) is acyclic \hspace{3cm} (internal/sc-per-loc)

ob is irreflexive \hspace{3cm} (external)

\(rmw \cap (fre; moe) = \emptyset\) \hspace{3cm} (atomicity)
Exercise

(1) Study the examples w.r.t ARMv8 model from:

- 'A Tutorial Introduction to the ARM and POWER Relaxed Memory Models’.

- ’Herding cats: Modelling, Simulation, Testing, and Data-mining for Weak Memory’. 