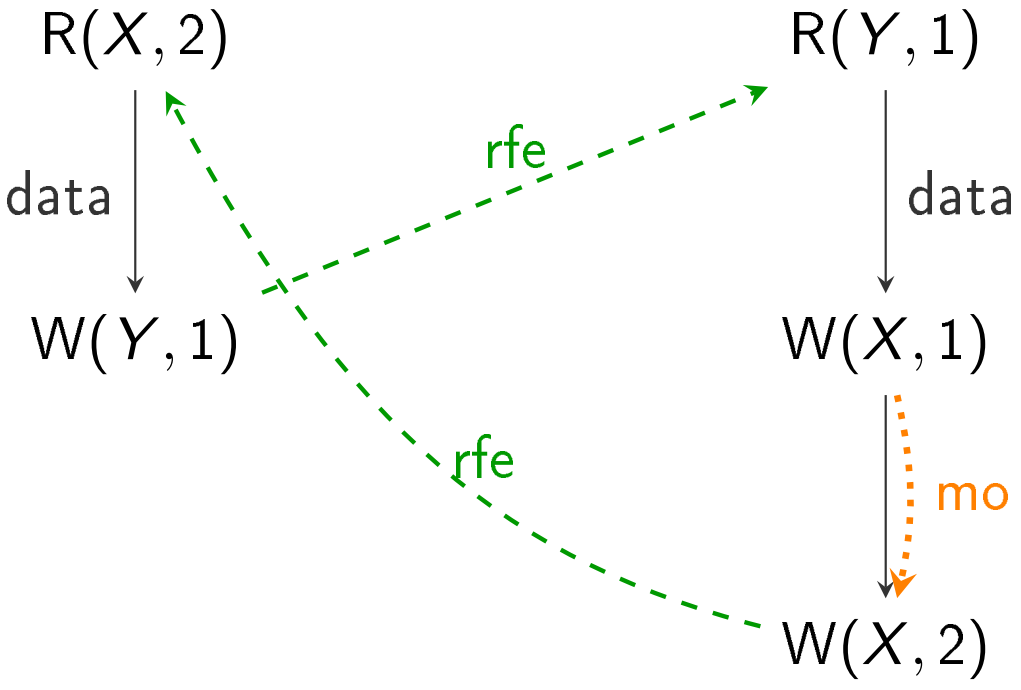
ARMv8 Architecture

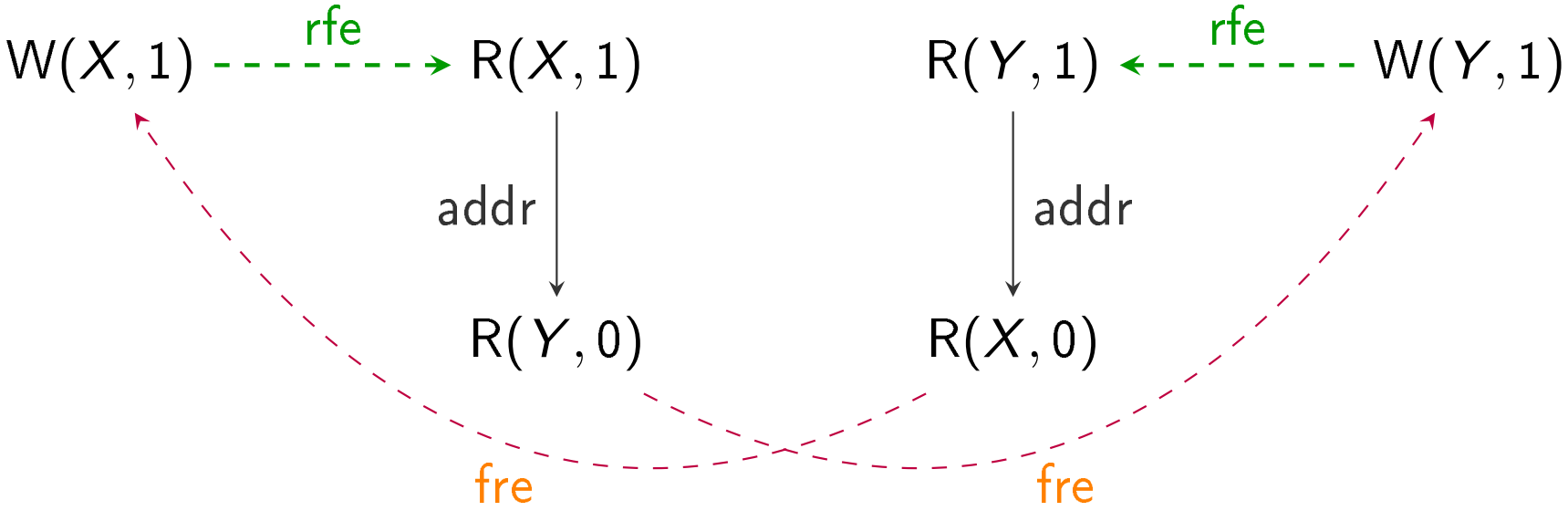
Some Observations from ARMv7

Non-intuitve behaviors.



Some Observations from ARMv7

Non-multicopy atomic behavior



Major Changes

Simplified ARM model.

- Removes non-multicopy atomicity.

Introduce stronger memory accesses and weaker fences

Additional memory accesses:

- Release-store: STLR (L)
- Acquire-load: LDAR (L)

Additional Fences:

- Load DMB (dmbld)
- Store DMB (dmbst)

Rules of New Primitives

STLR and LDAR constrains data access movement

- Accesses before an STLR are 'barrier-ordered-before' the STLR
- LDAR is 'barrier-ordered-before' following accesses
- STLR is 'barrier-ordered-before' following LDAR

Fence Rules:

- dmbfull is a full fence
- dmbld orders a load (R) with a following load (R) or store (W)
- dmbst orders a store (W) with a following store (W)

ARMv8 Relations

Coherence-after: $ca = fr \cup mo$

Observed-by: $obs = rfe \cup fre \cup moe$

Dependency-ordered-before:

$$\begin{aligned} dob = & addr \cup data \\ & \cup ctrl; [W] \\ & \cup (ctrl \cup (addr; po)); [isb]; po; [R] \\ & \cup addr; po; [W] \\ & \cup (ctrl \cup data); moi \\ & \cup (addr \cup data); rfi \end{aligned}$$

ARMv8 Relations

Atomic-ordered-before: $\mathsf{aob} = \mathsf{rmw} \cup [\mathsf{range}(\mathsf{rmw})]; \mathsf{rfi}; [A]$

Barrier-ordered-before:

$$\begin{aligned}\mathsf{bob} = & \mathsf{po}; [\mathsf{dmbfull}]; \mathsf{po} \\ & \cup [\mathsf{L}]; \mathsf{po}; [\mathsf{A}] \\ & \cup [\mathsf{R}]; \mathsf{po}; [\mathsf{dmbld}]; \mathsf{po} \\ & \cup [\mathsf{A}]; \mathsf{po} \\ & \cup [\mathsf{W}]; \mathsf{po}; [\mathsf{dmbst}]; \mathsf{po}; [\mathsf{W}] \\ & \cup \mathsf{po}; [\mathsf{L}] \\ & \cup \mathsf{po}; [\mathsf{L}]; \mathsf{coi}\end{aligned}$$

Ordered-before: $\mathsf{ob} = (\mathsf{obs} \cup \mathsf{dob} \cup \mathsf{aob} \cup \mathsf{bob})^+$

ARMv8 Axioms

$(po_x \cup \mathsf{fr} \cup \mathsf{mo} \cup \mathsf{rf})$ is acyclic (internal/sc-per-loc)

ob is irreflexive (external)

$\mathsf{rmw} \cap (\mathsf{fre}; \mathsf{moe}) = \emptyset$ (atomicity)

Exercise

(1) Study the examples w.r.t ARMv8 model from:

- *'A Tutorial Introduction to the ARM and POWER Relaxed Memory Models'*.

- *'Herding cats: Modelling, Simulation, Testing, and Data-mining for Weak Memory'*.