PowerPC Architecture
\[ \text{prop}_2 \triangleq (\text{moe} \cup \text{fre})?; \text{rfe}?; (\text{fence}; \text{hbp}^*)?; \text{hwsync}; \text{hbp}^* \]
\[
\text{prop}_2 \triangleq (\text{moe} \cup \text{fre})?; \text{rfe}?; (\text{fence}; \text{hbp}^*)?; \text{hwsync}; \text{hbp}^*
\]

Finally \( \text{prop} \triangleq \text{prop}_1 \cup \text{prop}_2 \)
Atomicity

Load-Linked (LL) and Store-Conditional (SC) provides atomicity.

Example. Atomic Add (Fetch and Add)

\[
\text{do} \{
    r := \text{LL}(x);
    r := r + v;
\} \text{ while}(\neg \text{SC}(r, x));
\]

Relation \( rmw \subseteq [R]; p_{ox}; [W] \)
(po \cup rf \cup mo \cup fr) \text{ is acyclic.} \quad \text{(SC-PER-LOC)}

fre; prop; hbp^* \text{ is irreflexive.} \quad \text{(OBSERVATION)}

(mo \cup prop) \text{ is acyclic.} \quad \text{(PROPAGATION)}

rmw \cap (fre; moe) = \emptyset. \quad \text{(ATOMICITY)}

hbp \text{ is acyclic} \quad \text{(NO-THIN-AIR)}
ARMv7 Architecture

Many similarities with PowerPC
MemoryAccesses:
Load, Store, Update (LL/SC pair)

Fence

- ARMv7 dmb $\iff$ PowerPC hwsync
- ARMv7 isb $\iff$ PowerPC isync

Differences

1. ARMv7 has no corresponding fence as PowerPC lwsync.
2. Same-location read followed by write does not ensure preserved-program-order in ARMv7.

$R_x; po; W_x \not\subseteq ppo$
Differentiating Example

\[ a = 1 \text{ is allowed in ARMv7 but not in PowerPC (why?)} \]

\[ a := X; \quad // \ 1 \quad \parallel \quad Y := X; \quad \parallel \quad X := Y; \]

\[
\begin{align*}
R(X, 1) & \quad R(X, 1) & \quad R(X, 1) \\
\downarrow & \quad \downarrow & \quad \downarrow \\
W(X, 1) & \quad W(Y, 1) & \quad W(X, 1)
\end{align*}
\]
Exercise

(1) Study the examples in PowerPC and ARMv7 models from:
- ’A Tutorial Introduction to the ARM and POWER Relaxed Memory Models’.
- ’Herding cats: Modelling, Simulation, Testing, and Data-mining for Weak Memory’.