PowerPC Architecture
Happens-before $hbp \triangleq rfe \cup \text{fence} \cup \text{ppo}$

(no-thin-air) Happens-before($hbp$) is irreflexive.

Example: $X = Y = 1$ is forbidden due to $hbp$ cycle.

\[
\begin{align*}
\text{if}(X == 1) & \quad | \quad \text{if}(Y == 1) \\
Y := 1; & \quad | \quad X := 1;
\end{align*}
\]

\[
\begin{array}{c}
\text{R}(X, 1) \\
\text{ctrl} \downarrow \\
W(Y, 1)
\end{array}
\quad \quad \\
\quad \\
\begin{array}{c}
\quad \text{rfe} \\
\quad \text{rfe}
\end{array}
\quad \\
\begin{array}{c}
\text{R}(Y, 1) \\
\text{ctrl} \downarrow \\
W(X, 1)
\end{array}
\]

\[
\begin{array}{c}
\text{rfe} \\
\text{rfe}
\end{array}
\]
Happens-before $\text{hbp} \triangleq \text{rfe} \cup \text{fence} \cup \text{ppo}$

(no-thin-air) Happens-before(hbp) is irreflexive.

Example: $a = 1$ is forbidden due to hbp cycle.

$$a := X; \quad // \quad 1$$
$$F_{\text{lwsync}};$$
$$Y := 1;$$
$$\text{if}(Y == 1) \quad Z := 1;$$
$$\text{if}(Z == 1) \quad X := 1;$$
Propagation Order

A partial order in which writes are propagated to memory.

Enforced by fences.

Propagation relation: \( \text{prop} \triangleq \text{prop}_1 \cup \text{prop}_2 \)

\( \text{prop}_1 \triangleq [W]; \text{rfe}^?; \text{fence}; \text{hbp}^*; [W] \)
\( \text{prop}_1 \triangleq [W]; \text{rfe}^2; \text{fence}; \text{hbp}^*; [W] \)
Exercise

Consider the examples from:
'A Tutorial Introduction to the ARM and POWER Relaxed Memory Models'.

In the respective execution graphs:
- Identify prop\(_1\) relations.
- Identify hbp relations.