Sanjana Singh

Ph.D.

Computer Science & Engineering

Indian Institute of Technology Delhi

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Gender: Female
D.O.B: 29/06/1990
Pronouns: She/Her

EDUCATION

- Indian Institute of Technology Delhi
  Ph.D. ***9.2 GPA*** *2016-2023*
  Under supervision of Subodh Sharma, Department of Computer Science and Engineering, IITD, on *Program analysis of weak memory concurrency*.
- Jaypee Institute of Information Technology, Noida *2008-2013*
  Integrated **B.Tech + M.Tech** (Computer Science and Engineering) ***80%***

RESEARCH INTERESTS

concurrency • program analysis • verification • model checking • weak memory models • efficiency

CODING SKILLS

C, C++, Python

Java, OCaml

LLVM, Clang

HTML, PHP

OpenMP, MPI, CUDA

OTHER TECHNICAL SKILLS:

Coq theorem prover, SAT, SMT, weak memory models (TSO, PSO, ARM, C/C++ and its variants)

REFERENCES:

1. Subodh Sharma
   Associate Professor, IIT Delhi
   svs@cse.iitd.ac.in
2. Sanjiva Prasad
   Professor, IIT Delhi
   sanjiva@cse.iitd.ac.in

ABOUT ME and OBJECTIVE

I embody discipline, dedication, and a strong work ethic. I have experience in both autonomous and team-based research, spanning the entire spectrum from conceptualization and design to implementation, testing, and performance evaluation. My problem-solving skills are characterized by creativity. Pursuing Ph.D. has instilled in me resilience and perseverance, along with improved patience and multitasking abilities.
I am enthusiastic about contributing my knowledge and expertise in research and problem solving towards the development of pragmatic and impactful solutions that can make a meaningful difference.

WORK EXPERIENCE

- Indian Institute of Technology Delhi *2016-2020*
  Teaching Assistantship
- Kobayashi Lab at University of Tokyo, Japan *2017*
  3 weeks under Japan-Asia Youth (Sakura Science) Exchange Program
- Jaypee University of Information Technology, Solan *2013-2016*
  Assistant Professor, T&P CSE head, and Curator/In-charge of CSE tech. club
- Bharti Airtel Ltd., Gurgaon (*Designation: Summer Intern*) *2011*

PUBLICATIONS

- Stateless Model Checking based on View-equivalence
  (*under revise and resubmit for* OOPSLA)
  Novel and coarsest equivalence, novel representative for execution sequences, sound, complete, and optimal model checkering, outperforms state-of-the-art.
  Independent work from conception to design, implementation, and benchmarking.
- Fence Synthesis Under the C11 Memory Model (ATVA 2022, Beijing, China)
  1st C11 automated repair using fences, optimal & scalable approaches, open source.
  Lead role in design, implementation, and benchmarking.
- Dynamic Verification of C11 Concurrency over Multi Copy Atomics (TASE 2021, Shanghai, China)
  Bridges developer and architecture (eg. x86 and ARM) specifications, novel fragment of C11 memory model, sound and precise model checking.
  Independent work in design, primary role in implementation and benchmarking.
- A novel approach for bug localization for Exception Handling and Multithreading through mutation (INDICON 2015, New Delhi, India)
  Uses killed mutations to detect potential bugs, specific support for richer constructs.
  Independent role in design, implementation, and testing.

PROJECTS

- Software Source-Code Analysis Related to Plagiarism Dispute for the Hon'ble Delhi High Court.
  Lead role in similarity and plagiarism detection, and technical report generation.
- Automated Bug Detection and Repair in C11 Programs: Insights and Experiences (*under peer review*)
  Performance and applicability analysis of state-of-the-art techniques, previously unreported technique insights, effective improvements proposed.
  Lead role in survey, testing, analysis, independent work on improvements.
- Extension of Stateless Model Checking based on view-equivalence for RA Memory Models. (*ongoing*)
  Independent work in design, support role for implementation and benchmarking.
- Lock-aware extension of Optimal Stateless Model Checking based on view-equivalence. (*ongoing*)
  Lead role in design, support in implementation and benchmarking.
- Mining developer mailing list for best fit query response (*B.Tech. Project*)
- Website design for 2nd Indian SAT+SMT school and Vertecs², IIT Delhi

TECHNICAL TALKS

- FMI Update Meeting, Goa, India *Jul 2023*
- SERI Update Meeting, Goa, India *Jun 2023*
- ATVA, Beijing, China *Oct 2022*
- TASE, Shanghai, China *Aug 2021*
- INDICON, New Delhi, India *Dec 2015*

EVENTS ORGANIZED

- 2nd Indian SAT+SMT School, Mysore, India (*organizer support*) *Dec 2017*
- 3rd IEEE ICIIP Solan, India *Dec 2015*
- 3rd IEEE PDGC, Solan, India *Dec 2014*
- 2nd IEEE ICIIP Solan, India *Dec 2013*