SANJANA SINGH

Ph.D.

Computer Science and Engineering
Indian Institute of Technology Delhi

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RESEARCH INTERESTS

Concurrency | Program Analysis | Verification | Model Checking | Weak Memory Models | Efficiency

ABOUT ME and OBJECTIVE

I embody discipline, dedication, and a strong work ethic. I have experience in both autonomous and team-based research, spanning the entire spectrum from conceptualization and design to implementation, testing, and performance evaluation. My problem-solving skills are characterized by creativity. Pursuing Ph.D. has instilled in me resilience and perseverance, along with improved patience and multitasking abilities.

I am enthusiastic about contributing my knowledge and expertise in research and problem solving towards the development of pragmatic and impactful solutions that can make a meaningful difference.

EDUCATION

Ph.D. *2016-2023*
Indian Institute of Technology Delhi *9.2 GPA*

Under supervision of Subodh Sharma, Department of Computer Science and Engineering, IITD

Dissertation Title: Program Analysis under Relaxed Memory Concurrency

Research keywords: model checking, dynamic and static program analysis, concurrency, weak memory models, sound and optimal analysis, efficient (scalable and performant) techniques, and effective implementations.

Integrated B.Tech + M.Tech in Computer Science and Engineering *2008-2013*
Jaypee Institute of Information Technology, Noida *7.6 GPA*

M.Tech. Dissertation Title: Bug localization for Exception Handling and Multithreading through mutation.

B.Tech. Major Project Title: Mining developer mailing list for best fit query response

PUBLICATIONS

Stateless Model Checking based on View-equivalence *under revise and resubmit for* OOPSLA, 2023

Highlights: Novel and coarsest equivalence relation. Novel representative for execution sequences. Sound, complete, and optimal model checking. Accompanying tool outperforms state-of-the-art, open-source (to be released on publication).

Roles: Independent work from conception to design, implementation, and performance evaluation.

Fence Synthesis Under the C11 Memory Model ATVA 2022, Beijing, China

Highlights: 1st automated repair under C11 using fences. Optimal & scalable approaches. Open-source.

Roles: Lead in design, implementation, and performance evaluation.

Dynamic Verification of C11 Concurrency over Multi Copy Atomics TASE 2021, Shanghai, China

Bridges developer and architecture (eg. x86 and ARM) memory model specifications. Novel fragment of C11 memory model. Sound and precise model checking.

Roles: Independent work in design, primary role in implementation and performance evaluation.

A novel approach for bug localization for Exception Handling and Multithreading through mutation INDICON 2015, New Delhi, India

Highlights: Uses killed mutations to detect potential bugs. Specific support for richer constructs.

Roles: Independent work from conception to design, implementation, and testing.

ONGOING RESEARCH PROJECTS

Automated Bug Detection and Repair in C11 Programs: Insights and Experiences (*under peer review*)

Highlights: Performance and applicability analysis. Focus on state-of-the-art Bug Detection and Repair techniques for C11. Previously unreported technique insights. Effective improvements proposed.

Roles: Lead in survey, testing, analysis, independent work on improvements.

Optimal Stateless Model Checking based on View-equivalence for RA memory model

Highlights: Coarsest stateless model checking under RA. Sound and complete. Model checking for read-world (non-theoretic) memory model. Accompanying open-source tool (to be released on publication).

Roles: Independent role in design, support in implementation and performance evaluation.

Lock-aware Optimal Stateless Model Checking based on View-equivalence

Highlights: Support for richer constructs under coarsest exiting equivalence relation. Sound, complete, and optimal stateless model checking. Accompanying open-source tool (to be released on publication).

Roles: Lead in design, primary role in implementation and performance evaluation.

OTHER PROJECTS

Software Source-Code Analysis Related to Plagiarism Dispute for *the Hon'ble Delhi High Court*

Roles: Lead in similarity and plagiarism detection, and technical report generation.

Website design for The Second Indian SAT+SMT School, Mysore, India

Website design for Vertecs^2 research group at IIT Delhi

TEACHING EXPERIENCE

Teaching Assistant *2016-2020*

Indian Institute of Technology Delhi *New Delhi, India*

Roles: Management and guidance on Graduate and Undergraduate projects, Lectures, Lab setup, Assignment design and infrastructure setup, Grading.

Assistant Professor *2013-2016*
Jaypee University of Information Technology *Solan, India*

Roles: Research, Lectures, Tutorials, Course and Lab design and setup, Grading, Management and guidance on undergraduate projects, various administrative duties.

Other designations: i. Training and Placement CSE head, and
ii. Curator and Faculty in-charge of CSE technical club "Enkindle"

INTERNSHIPS

Exchange Research Intern *Jun 2017 – July 2017*
University of Tokyo *Tokyo, Japan*

3 weeks under Japan-Asia Youth (Sakura Science) Exchange Program in Kobayashi Lab.
Role: Research exchange leading to collaborations

Summer Intern *May 2011 – June 2011*
Bharti Airtel Ltd. *Gurgaon, India*

Role: Assistance on routers installation.

TECHNICAL PRESENTATIONS / TALKS

Formal Methods India Update (FMU) Meeting 2023, Goa, India *Jul 2023*

Title: Optimal Stateless Model Checking based on View-equivalence

Software Engineering Research in India (SERI) Update Meeting 2023, Goa, India *Jun 2023*

Title: Fence Synthesis under the C11 Memory Model

20th International Symposium on Automated Technology for Verification and Analysis (ATVA), Beijing, China (attended virtually) *Oct 2022*

Title: *Fence Synthesis Under the C11 Memory Model*

15th Theoretical Aspects of Software Engineering Conference (TASE), Shanghai, China (attended virtually) *Aug 2021*

Title: Dynamic Verification of C11 Concurrency over Multi Copy Atomics

12th Annual IEEE India Conference (INDICON), New Delhi, India *Dec 2015*

Title: A novel approach for bug localization for Exception Handling and Multithreading through mutation

CONFERENCES and WORKSHOPS ORGANIZED

The Second Indian SAT+SMT School, (*Organization support*), Mysore, India *Dec 2017*

IEEE Third International Conferences on Image Information Processing (ICIIP), Solan India *Dec 2015*

IEEE Third International Conference on Parallel, Distributed and Grid Computing (PDGC) Solan India *Dec 2014*

IEEE Second International Conferences on Image Information Processing (ICIIP), Solan India *Dec 2013*

WORKSHOPS ATTENDED

The Third Indian SAT+SMT School, Hyderabad, India — *Dec 2018*

Winter School in Software Engineering, Pune, India — *Dec 2017*

The Second Indian SAT+SMT School, Mysore, India — *Dec 2017*

The First Indian SAT+SMT School, Mumbai, India — *Dec 2016*

FUTURE RESEARCH GOALS

Scalable program analysis

Scalable approaches capable of efficiently handling large programs. May leverage symbolic execution, integrate machine learning, or utilize parallelization, while ensuring a satisfactory quality of results.

Application of program analysis techniques to other programming paradigms

Paradigms including concurrent data structures, database transactions, distributed systems, and neural nets.

Synthesis under relaxed models

Specifically, automated correction of bugs induced by relaxed semantics and automated transformations that optimize the utilization of relaxed ordering.

TECHNICAL SKILLS

Coding Skills:

C/C++ Python

Java OCaml

LLVM Clang

HTML PHP JS CSS

OpenMP MPI CUDA

Other Technical Skills:

Coq Theorem Provers | SAT and SMT solvers | Weak Memory Models (multi/non-multi)-copy atomicity

Weak Memory Models: TSO, PSO, ARM, Power, RISK-V, C11-style including C11, RCxx, (s/w/)RA.

LANGUAGES

English — *Fluent Professional Proficiency*

Hindi — *Native*

PERSONAL DETAILS

Gender: Female
D.O.B: 29/06/1990
Pronouns: She/Her

References:

Subodh Sharma
Associate Professor, IITD
svs@cse.iitd.ac.in

Sanjiva Prasad
Professor, IITD
sanjiva@cse.iitd.ac.in

S.Arun Kumar
Professor, IITD
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