Neeraj Goel

Department of Computer Science,
IIT Delhi, Hauz Khas,
New Delhi 110016
Phone No: 91 11 2659 6049(Lab)
Fax No: 91 11 2658 6010

Email: neeraj@cse.iitd.ernet.in
Home: http://www.iitd.ernet.in/~neeraj

Objective I am a PhD student working with Embedded System Group in Department of Computer Science and Engg at IIT Delhi. Key interests of my research are exploration of memory hierarchy for high issue rate processors such as VLIW. I am also interested in the tools and compilers related to VLIW/ EPIC domain of processors. I am an M Tech in VLSI Design Tool & Technology from IIT Delhi and my final M Tech project was hardware/software co-design of a face detection algorithm.

Education

Indian Institute of Technology Delhi — New Delhi
July 2004 – Current
Phd Student
Current CGPA 8.3 in scale of 10
Dissertation Area : Memory hierarchy exploration for VLIW ASIPs
Supervisors : Dr Preeti Ranjan Panda and Prof Anshul Kumar

Indian Institute of Technology Delhi — New Delhi
2002–2004
M Tech in VLSI Design Tool and Technology
CGPA 8.43 in scale of 10

Regional Engg Collage Kurukshetra — Kurukshetra
1998–2002
B Tech in Electronics and Communication
Aggregate 71.4%

Ongoing Work

Literature Survey: Reading and analysis of the work that has been done in my area of dissertation

Modeling Caches: Modeling the behavior of the cache in multi-cluster environment. Accurate models are necessary for designing better memory hierarchy

Code Generation: Extending existing framework of trimaran compilers for clustered VLIW processors. Code generation for clustered VLIW will serve as platform for performing all the experiments needed to carry out research.

Work Experience

Philips Research — Eindhoven, The Netherlands
Feb 2004 – May 2004

Worked with 'Embedded System Architecture on Silicon' (ESAS) group. Work assigned was the analysis of a face detection algorithm then finding suitable architecture for implementation in a mobile domain application. Issues involved were to get the real time solution of the problem with given architectural and QoS constraints. Methodology used was hardware software co-design of the algorithm.

IIT Delhi — New Delhi
2002 – current

TA to Prof M Balakrishnan for Digital Hardware Design Lab and High level System Design Lab,
TA to Prof B. Bhaumik for Electronics Lab course.
Responsibilities include to instruct, guide and evaluate students.

Projects

Partial Reconfiguration of Xilinx FPGA: Project including demonstrating run time reconfiguration capabilities of Xilinx FPGA. The work was novice as no body in our knowledge has done it so far for a big application. Further it includes a quantitative analysis of overhead of reconfiguration. *Published in VDAT 2005, held on 11-13 August in Banglore*

Analysis of a face tracking algorithm for embedded implementation The project aims at improvement in the speed of face tracking for real time application. The project include study of various algorithms of face tracking, selection of an algorithm, analysis of that algorithm, implementation of the algorithm. Then analyzing the implementation for embedded implementation. In this study we have to profile the C code with different tools and the find the parts of the algorithm suitable for hardware implementation. Further, his is the first step for architecture exploration for doing implementation.

Voice recognition system This system, which was designed in MATLab, uses the inherent qualities of a speaker's voice which helps in identifying the speaker.

Cache Design: Designed layout of a 256kb, 2-way associative Instruction Cache in 0.18u UMC fabrication technology using Cadence Design tools. This was a group project and my part was to look at architectural level issues and designing floorplan, decoders, comparators

Power Estimation for VLIW: Involved in the work that aims at instruction level power estimates for VLIW processor and generates power profile for any application

Designed and modeled an **Automatic Electric Power Measuring System** in SystemC.

Implemented an 8 bit **High Speed Current Steering DAC** in Tanner tool set.

Modeled a **Cycle accurate model of processor 8085 in VHDL** and simulated in Modelsim

Achievements

Job offer from Motorola in July 2004

Recipient of Philips Scholarship during M.Tech (July 2002 - May 2004)

All India Rank 16 in GATE 2002 with percentile 99.92 in EC

All India Rank 41 out of 40,000 students in CEET (Common Engineering Entrances Exam.) conducted by Kurukshetra University Kurukshetra in year 1998.

Recipient of Harayana State Board scholarship during 1996-1998.

Computer Skills

Operating System Dos, Windows, Linux, Solaris
Programming Language 'C', C++
System/Hardware Description Language VHDL, SystemC
VLSI Related Tools Xilinx ISE, Mentor's Modelsim, Synplify Synthesis tool, Tanner tool suit, FPGA Express

References

Prof M Balakrishnan
Department of Computer Science,
IIT Delhi

Prof Anshul Kumar
Department of Computer Science
IIT Delhi

Dr Preeti Ranjan Panda
Department of Computer Science
IIT Delhi