



ACADEMIC DETAILS

Year	Degree / Exam	Institute	GPA / Marks(%)
----	M.Tech in VLSI Design, Tool & Technology	Indian Institute of Technology Delhi	7.941
2002	Board of Higher Secondary Examination, Kerala	ASMMHSS, Alathur, Kerala	81.77%
2000	General Education Department, Kerala	SMMHS, Pazhambalacode, Kerala	88.5%

DEGREES PRIOR TO IIT

University	Examination	GPA / Marks(%)
Nehru College of Engg. & Research Center, Thrissur, Kerala (University of Calicut) (2002-2006)	B.Tech	76.46%

COURSES DONE

Data Structures And Algorithms , Arch.of Large Systems , Synthesis Of Digital Systems , System Level Design And Modelling , Approximation Algorithms* , Digital Systems Lab. , Microelectronics* , Mos Vlsi , Ic Technology , Computer Aided Vlsi Design , Ic Processing Lab , Major Project Part-i* , Independent Study* .

* Courses currently pursuing

IIT DELHI THESIS

Title - Low Power Memory Architecture Inference in High Level Synthesis

Supervisor - Dr. Preeti Ranjan Panda (IIT Delhi), Srihari Y (Calypto Design Systems)

Description -Given the High Level HDL code of a hardware, the memory architecture has to be inferred automatically targetting low power designs. Standard Static Memory IP specifications will be used in order to do this. A Synthesis tool will be developed at the end of the course which generates the equivalent RTL code which will be analysed further with Calypto's PowerPro tool for power profiling. CatapultC Synthesis tool will be used in order to verify the feasibility of the proposed High Level to RTL flow.

QUALIFYING EXAMS

GATE Rank: 349/657 (GE)

WORK EXPERIENCE

- **Infosys Technologies Ltd., Bangalore** (July, 2006 - July, 2009) : Designation: Software Engineer. Worked in three locations of this organisation - Hyderabad, Bangalore and Trivandrum.
Project: Business Process Management for world's second largest auto parts dealer. Involved in Feasibility Analysis, Requirement Specification, Design and Development. Tool used: Tibco iProcess
Project: Enterprise Transport Management for One of the largest Beverages company. I was heading the testing team from the offshore center for around 8 months. I was also a member in Development and Quality Control team of the project. Tools/Technologies: Ab Initio, DML
Project: Enterprise Application Integration for world's second largest mining company. I was involved in Design and Development of 3 major interfaces of the project. Tools: SAP XI
Infosys Spot award for best performance in EAI Unit, when I was in a team of 30 (Sep, 2007)

PROJECTS

- **High Level Power Model of DDR3 SDRAM Based on Application Trace Samples** (Jan, 2010 - Present) : The Project targets High Level Power Modelling DDR3 SDRAM based on the application traces sampled by running different types of applications/benchmarks. A primitive level abstract model is already done during the first phase of the project. The second phase is ongoing.
- **High Level Power Optimization of DDR3 SDRAM Based on Application Trace Samples** (July, 2010 - Present) : The projects targets Power Optimization of DDR3 SDRAM based on a high level power model, by proposing a proper scheduling algorithm or by suggesting changes in hardware configuration inside the processor cores.
- **Scheduling Algorithm for Multiple Memory Controllers for High Performance & Low Power** (Jan, 2010 - May, 2010) : The project suggested a scheduling algorithm for multiple memory controller scenarios targetting low power and high performance. A SystemC model was developed and simulated extensively. The algorithm is mainly

- based on an already existing algorithm called ATLAS (Adaptive per-Thread Least Attained Scheduling).
- **Tool for Synthesizable VHDL Code (RTL) Generation** (July, 2009 - Dec, 2009) : This tool takes as input, the CDFG model of a high level VHDL description and generates the equivalent synthesized RTL code. The Scheduling and Register Allocation were annotated in the data structures manually. The purpose of the project was to automate the RTL generation assuming that the Scheduling and Register/Resource allocations are already done.
 - **Configurable Multicore Cache Simulator in SystemC** (Jan, 2010 - May, 2010) : This simulator models the 4-state Berkeley cache coherence protocol for multicore processors. The entire model was implemented in SystemC. The caches share a common bus where request/grant signals from each cache will content each other and thus gets resolved according to Berkeley protocol.
 - **Performance Evaluation - Binary Heap Vs Fibonacci Heap for Prim's Algorithm for Random Graphs** (July, 2009 - Dec, 2009) : The project included the performance evaluation of Prim's MST algorithm which uses either Fibonacci Heap or Binary Heap. High density random graphs (around 1 crore edges) were generated in order to prove that Fibonacci Heaps work better than Binary Heap for Prim's Algorithm. The running time was plotted and compared against each other.
 - **Adaptive Simulated Annealing Assistance for GOSAM (A Global Optimisation algorithm)** (Jan, 2010 - May, 2010) : The currently existing algorithm GOSAM is a global optimisation algorithm which uses Gradient Descent method for its local search. This was replaced by Adaptive Simulated Annealing algorithm in order to improve its local search capability and to reduce the no of iterations by making the whole process converge faster.
 - **4X4 Multiplier Design and Layout** (Oct, 2009 - Dec, 2009) : A 4X4 Multiplier was designed and the layout of the same was done in 130nm technology using UMC library. A standard cell of a NAND gate was also implemented as part of this.

TECHNICAL SKILLS

- C, C++
Markup Languages: HTML + CSS, XML, XSLT
HDL: VHDL, SystemC, Verilog
Scripting: Unix Shell Scripting
- Mentor Graphics CatapultC Synthesis, Xilinx ISE, Mentor Graphics ModelSim, SimpleScalar, Cadence ICFB, Synopsis Design Compiler, Cadence Conformal, Cadence Encounter

POSITIONS OF RESPONSIBILITY

- **Website Design & Maintenance, VDTT Website** (Jan, 2010 - Present) : I am responsible for maintaining the VDTT Website at present. This website was fully redesigned and renovated by me.
- **Placement Coordinator, VLSI Group at IIT Delhi** (Aug, 2010 - Present) : I am one of the two coordinators of the Track-4 Placement activities for VLSI group at IIT Delhi (Placements 2010). Responsibilities include Interaction with Industries, students, Prof. in-charge and TnP Cell - IIT Delhi
- **Vice President, Computer Science & Engg. Association, NCERC** (July, 2003 - July, 2004) : I was responsible for coordinating the association activities in the college.

OTHER INTERESTS

Music, Travel and Photography