Anup Gangwar

CONTACT INFORMATION

(Address omitted)

Voice: (omitted)
Mobile: (omitted)
E-mail: anup.gangwar@gmail.com
WWW: www.cse.iitd.ac.in/~ anup

RESEARCH INTERESTS

Embedded Systems and Architectures, VLIW Processors – Architectures, Compilers and Tools, Real Time Operating Systems, FPGA based design

EDUCATION

Indian Institute of Technology Delhi, New Delhi
Department of Computer Science and Engineering

Ph.D. in Computer Science and Engineering, July 2005

- *Dissertation Area:* "A Methodology for Exploring Communication Architectures of Clustered VLIW Processors"
- *Advisors:* Prof. M. Balakrishnan and Prof. Anshul Kumar

Indian Institute of Technology Delhi, New Delhi
Department of Computer Science and Engineering

M.Tech. in VLSI Design Tools and Technology (VDTT), December 2000
CGPA: 8.1/10.0

- *Thesis Title:* "Multi-processor Multi-tasking Performance Data Measurement and Visualization"
- *Advisors:* Prof. Anshul Kumar, Prof. M. Balakrishnan and Dr. Ir. Jos van Eijndhoven

Bhilai Institute of Technology, Bhilai
Department of Electrical Communication Engineering

B.E. in Electronics and Telecommunications, June 1998
Percentage: 71%

PROFESSIONAL EXPERIENCE

Freescale Semiconductors (I) Pvt. Ltd., NOIDA, India

FSL Software Engineer-III **Jul 2006 - present**
Working on various activities related to SoC bringup.

Calypto Design Systems (I) Pvt. Ltd., NOIDA, India

Sr. Member of Technical Staff **Nov 2004 - Jun 2006**
Worked on frontend aspects of various languages and also added a VHDL frontend to the Equivalence Checker Product, SLEC.

Philips Research Laboratories Eindhoven, Eindhoven, The Netherlands

Research Intern **Aug 2000 - Nov 2000**
Defined and implemented hooks inside simulator for *ECLIPSE*, Philips's next generation multi-media platform, for performance data measurement, analysis and visualization.

HONORS AND AWARDS

Receipent of 2007 ACM Transactions on Design Automation of Electronic Systems (TODAES) best paper award, for the paper titled, *"Impact of Intercluster Communication Mechanisms on ILP in Clustered VLIW Architectures"*.

Secured 99.28 percentile, AIR -38 in GATE-1998

Won the Computer Programming Contest organized by CSI in 1996

PUBLICATIONS

Anup Gangwar, M. Balakrishnan, Preeti Ranjan Panda and Anshul Kumar. "Evaluation of Bus Based Interconnect Mechanisms in Clustered VLIW Architectures", Springer International Journal of Parallel Programming (IJPP). *Accepted for Publication*

Anup Gangwar, M. Balakrishnan and Anshul Kumar. "Impact of Intercluster Communication Mechanisms on ILP in Clustered VLIW Architectures", ACM Transactions on Design Automation of Electronic Systems (TODAES). Vol. 12, No. 1, Jan 2007.

Ankit Mathur, Mayank Agarwal, Soumyadeb Mitra, Anup Gangwar, M. Balakrishnan, and Subhashis Banerjee. "SMPS: An FPGA-based Prototyping Environment for Multiprocessor Embedded Systems", IEEE/ACM Thirteenth International Symposium on Field Programmable Gate Arrays (FPGA-2005), Feb 2005, Monterey, USA. *(Poster Presentation)*

Anup Gangwar, M. Balakrishnan, Preeti Ranjan Panda and Anshul Kumar. "Evaluation of Bus Based Interconnect Mechanisms in Clustered VLIW Architectures", IEEE/ACM Design Automation and Test in Europe (DATE05), Mar 2005, Munich, Germany.

Anshul Kumar, M. Balakrishnan, Manoj Kumar Jain and Anup Gangwar, "Customizing Embedded Processors for Specific Applications", Recent Trends in Practice and Theory of Information Technology, Proceedings of NRB Seminar, Jan 2005, NPOL, Cochin, India

Anup Gangwar, M. Balakrishnan and Anshul Kumar. "Customizing Clustered VLIW Architectures with Focus on Interconnects and Functional Units", SIGDA Ph.D. Forum at 41^{st} IEEE/ACM Design Automation Conference (DAC-41), Jun 2004, San Diego, USA. *(Poster Presentation)*

Anup Gangwar, M. Balakrishnan and Anshul Kumar. "Impact of Inter-cluster Communication Mechanisms on ILP in Clustered VLIW Architectures", 2^{nd} Workshop on Application Specific Processors (WASP-2), in conjuction with 36^{th} IEEE/ACM Annual International Symposium on Microarchitecture (MICRO-36), Dec 2003, San Diego, USA

Amarjeet Singh, Amit Chhabra, Anup Gangwar, Basant K. Dwivedi, M. Balakrishnan and Anshul Kumar, "SoC Synthesis With Automatic Interface Generation", 16^{th} IEEE/ACM International Conference on VLSI Design (VLSI-2003), Jan 2003, New Delhi, India

Bhuvan Middha, Varun Raj, Anup Gangwar, Anshul Kumar, M. Balakrishnan and Paole Ienne, "A Trimaran Based Framework for Exploring Design Space of VLIW ASIPs With Coarse Grain Functional Units", 15^{th} IEEE/ACM International Symposium on System Synthesis (ISSS'02), Oct 2002, Kyoto, Japan

Anup Gangwar, Jos T. J. van Eijndhoven, M. Balakrishnan and Anshul Kumar, "Multi-Processor Multi-Tasking Performance Data Measurement and Visualization", Nat. Lab. (Philips Research Laboratories Eindhoven) Technical Note 2001/9, Jan 2001, Eindhoven, The Netherlands

PROJECTS

Details for each of these projects are available from: www.cse.iitd.ac.in/˜ anup

- ❑ *Multi-processor Extensions to LEON*
- ❑ *Synthesis and Testing of LEON Processor*
- ❑ *Segmentation Based Image Compression*
- ❑ *A framework for Studying Effects of VLIW Instruction Encoding Schemes*
- ❑ *Multi-processor Multi-tasking Performance Data Measurement and Analysis (M.Tech Project)*

COMPUTER SKILLS

- ❑ *Operating Systems:* Unices (Solaris, HP_UX, AIX, Linux), Windows
- ❑ *Programming Languages:* C, C++, Java (on UNIX)
- ❑ *Hardware Modeling Languages:* VHDL, SystemC
- ❑ *Other Languages:* Perl, Shell Scripting (Korn and clones with sed etc.)
- ❑ *Tools Used:* VLSI Design Tools: Synopsys-DC, Silicon Ensemble, Modelsim, FPGA Synthesis Tools: Synplify, FPGA Express etc.