TASE
2021

MoCA: Dynamic Verification of C/C++11 Concurrency over Multi-copy Atomics

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Indian Institute of Technology Delhi

Memory models

- *Interleaving*
- varying degrees of *Reordering*

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ARM
- interleaving
- all coherent reordering

C11 memory model

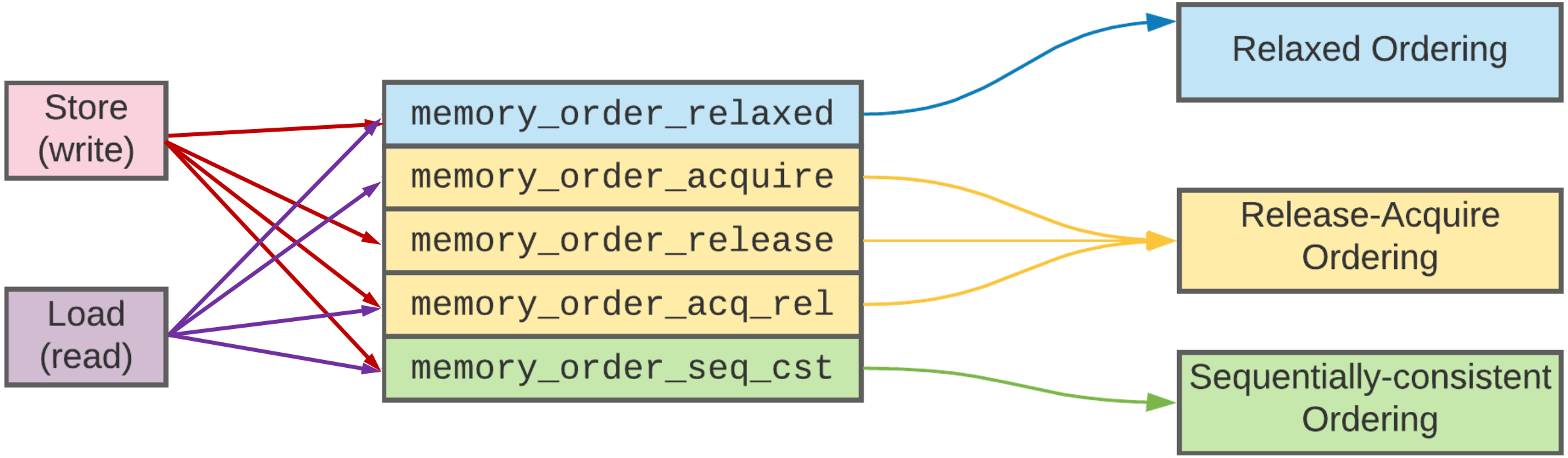
International
Organization for
Standardization

ISO

C++ 2011

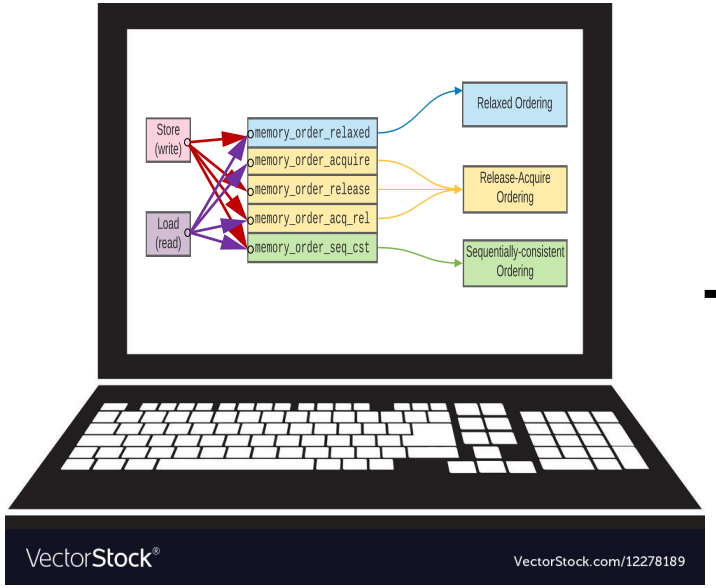
C11 memory model

International Organization for Standardization



https://www.cooldoger.com/2020/09

C11 memory model

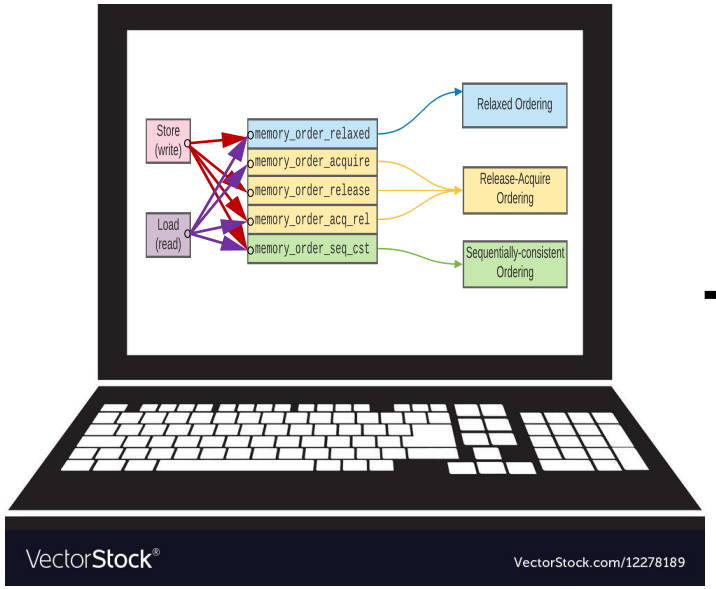


C/C++
Compiler

System
Architecture

$x{:=}1$	$y{:=}1$
barrier	*barrier*
$\mathrm{b}{:=}y$ (0)	$\mathrm{d}{:=}x$ (0)

C11 memory model



C/C++ Compiler

System Architecture

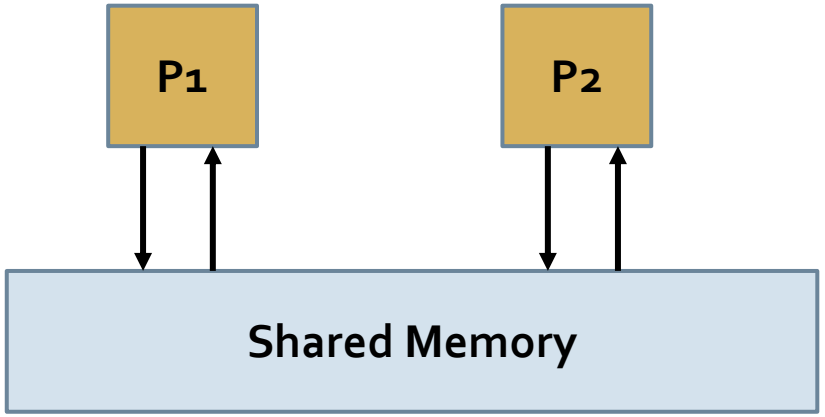
Axiomatic reasoning

reads-from relation (*rf*)
modification-order (*mo*)
Synchronizations (*sw*, *dob*)

$x{:=}1$	$y{:=}1$
barrier	*barrier*
$b{:=}y$ (0)	$d{:=}x$ (0)

Multi-copy Atomic model

- a single abstract view of shared memory



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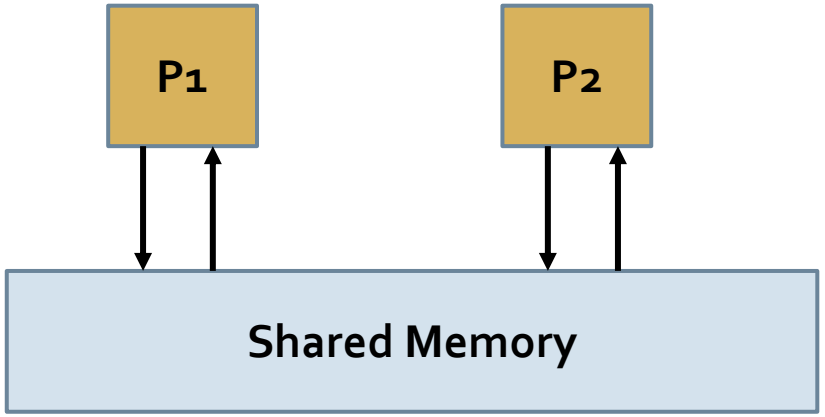

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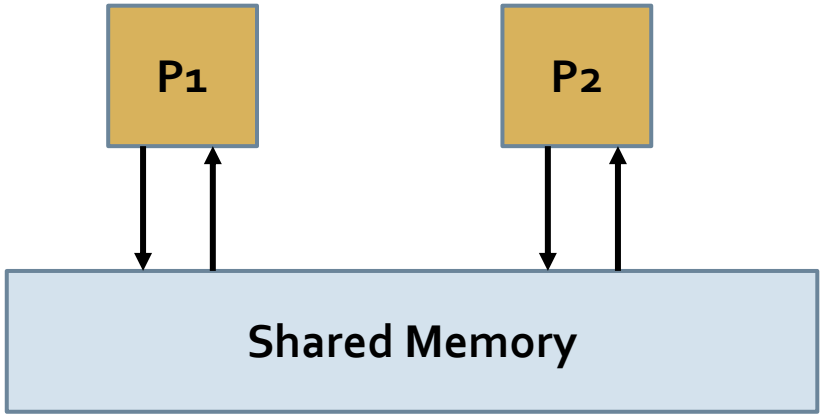

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ARM®
version 8 and later

α

x86

Multi-copy Atomic model

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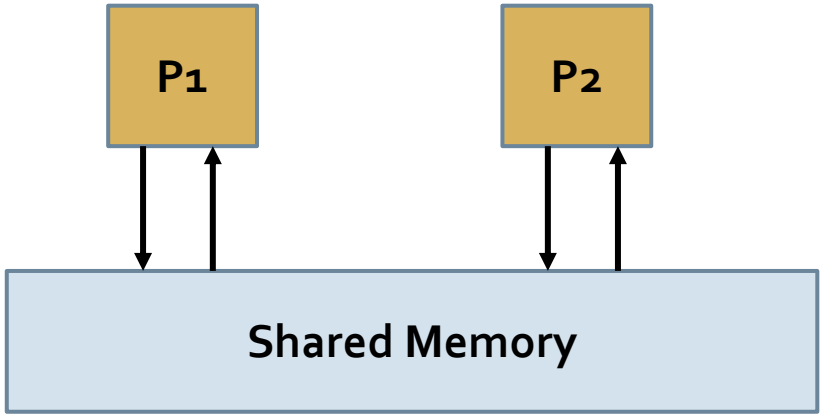

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T_1	T_2	T_3	T_4
$x:=1$	if $(x=1)$	$y:=1$	if $(y=1)$
	a:=y		b:=x

(IRIW)

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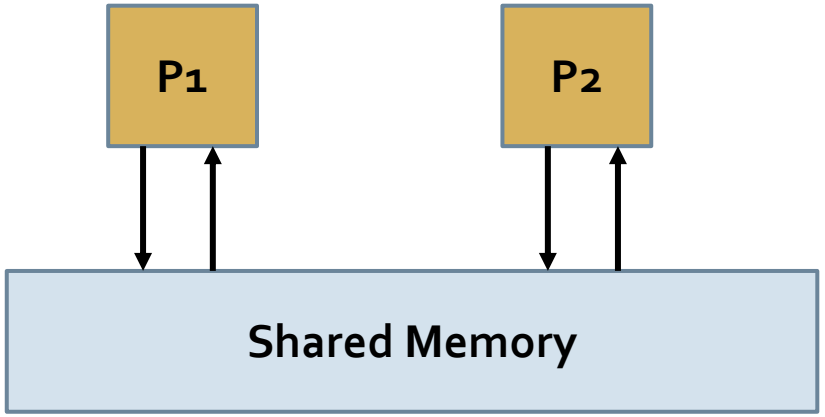

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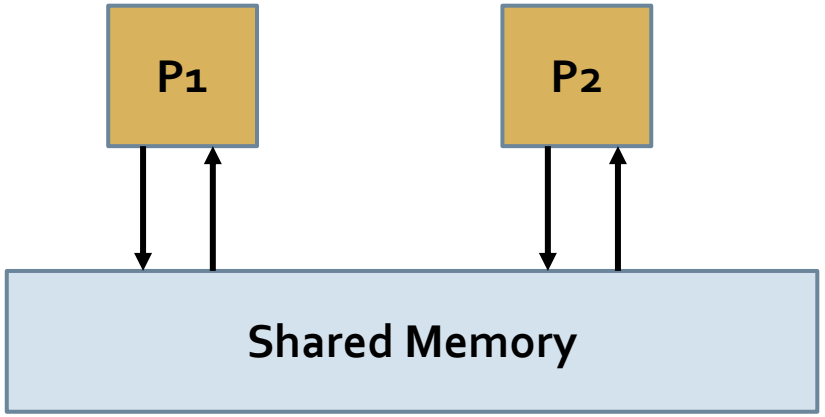

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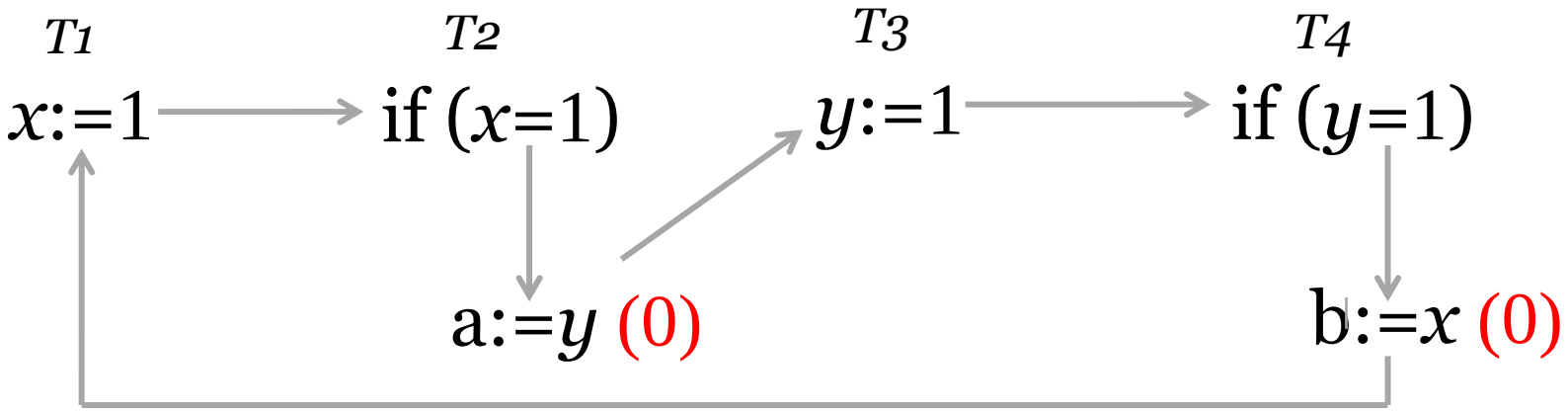
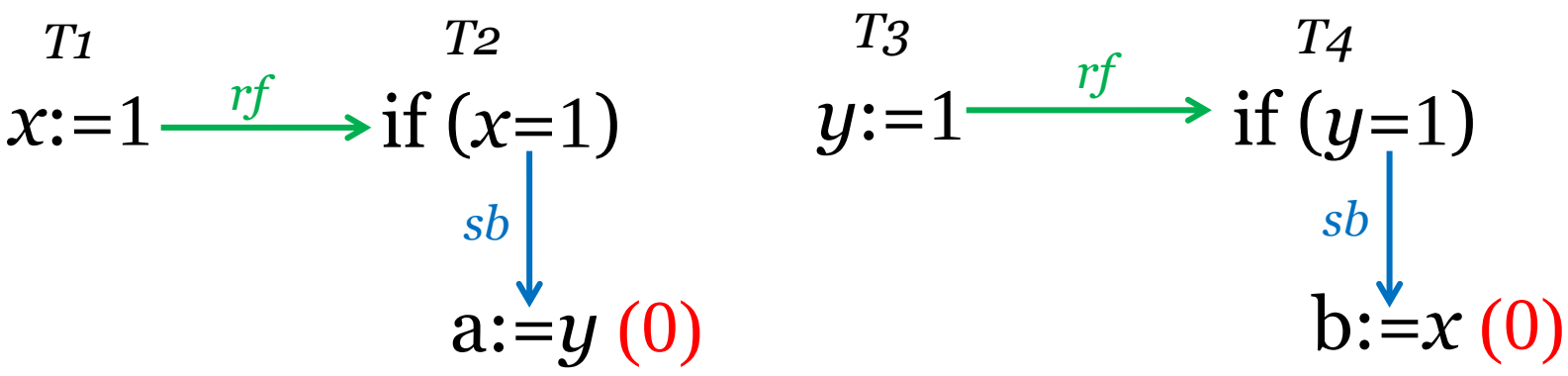


(IRIW)

C11 allows *non*-MCA

(IRIW) allowed under C11



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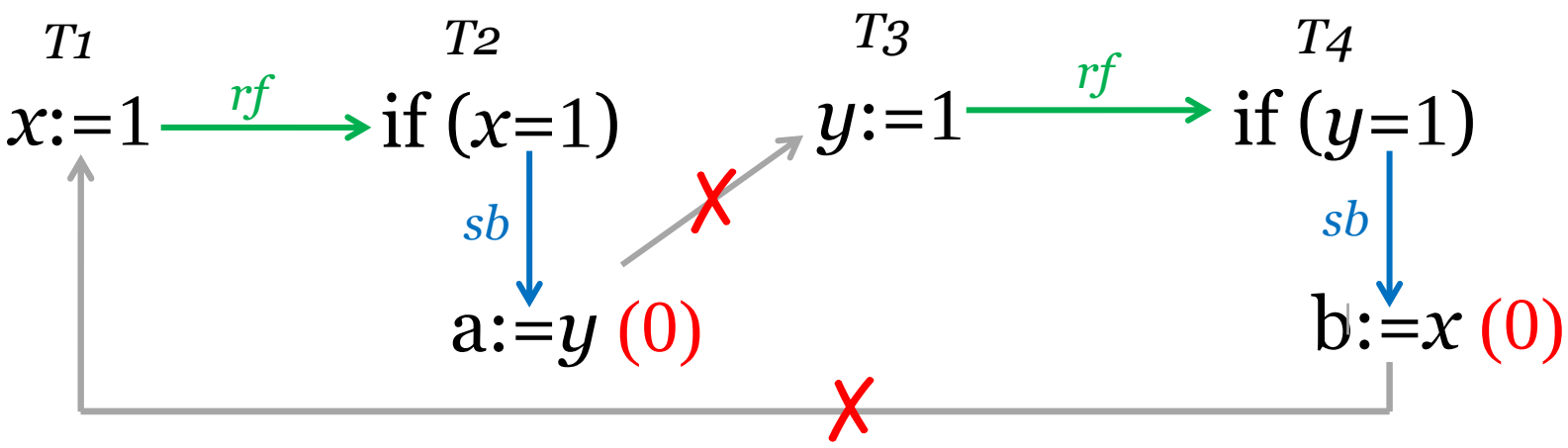

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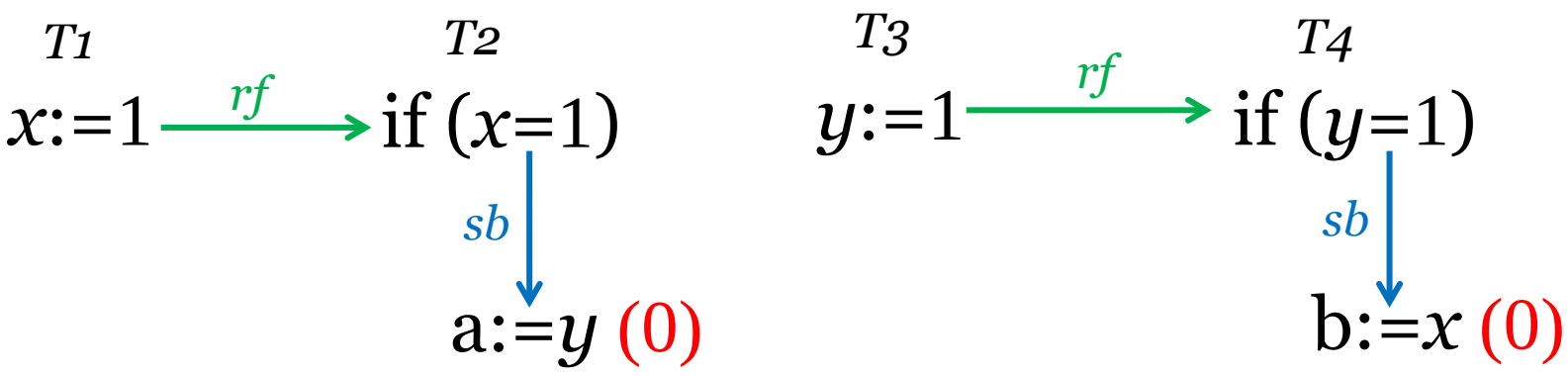
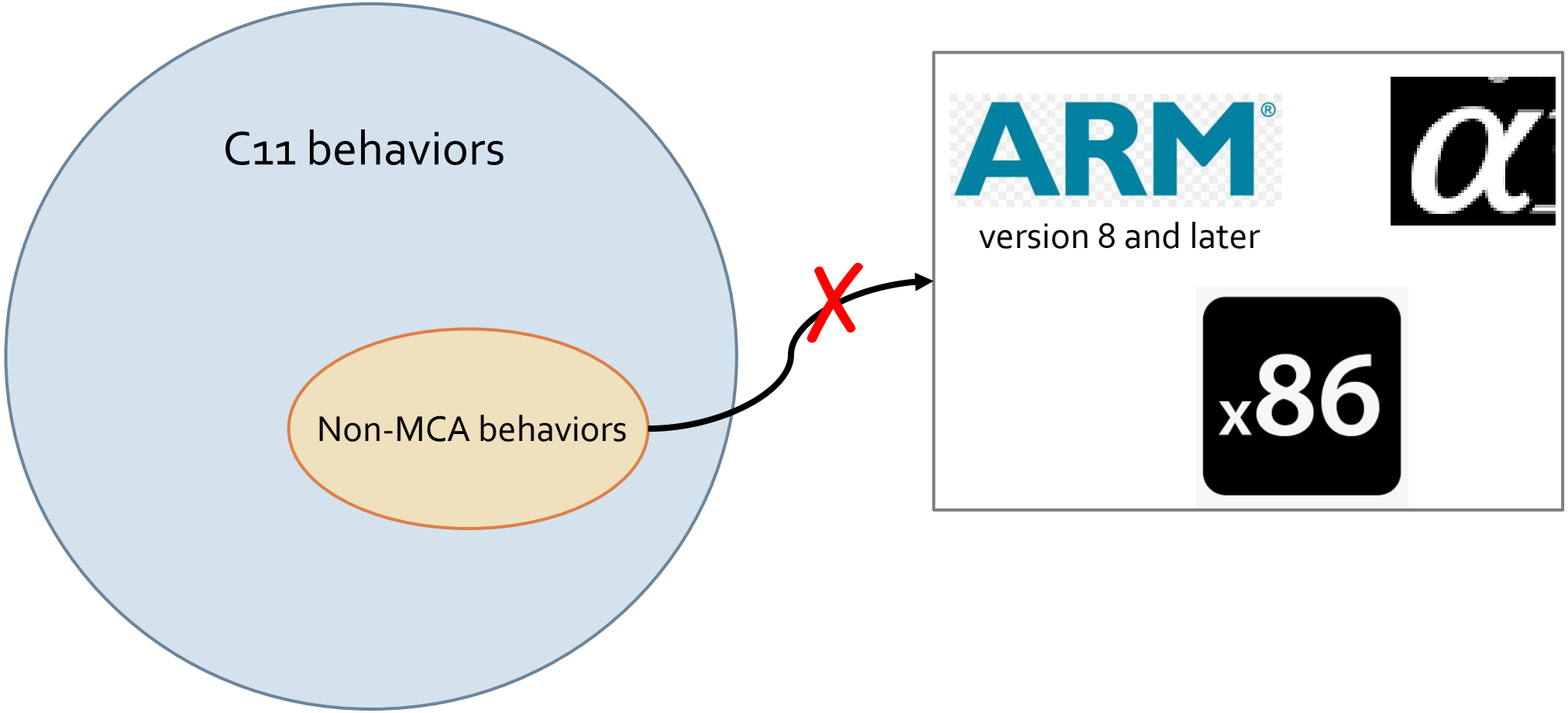


C11 over MCA

C11 over MCA -- *why?*



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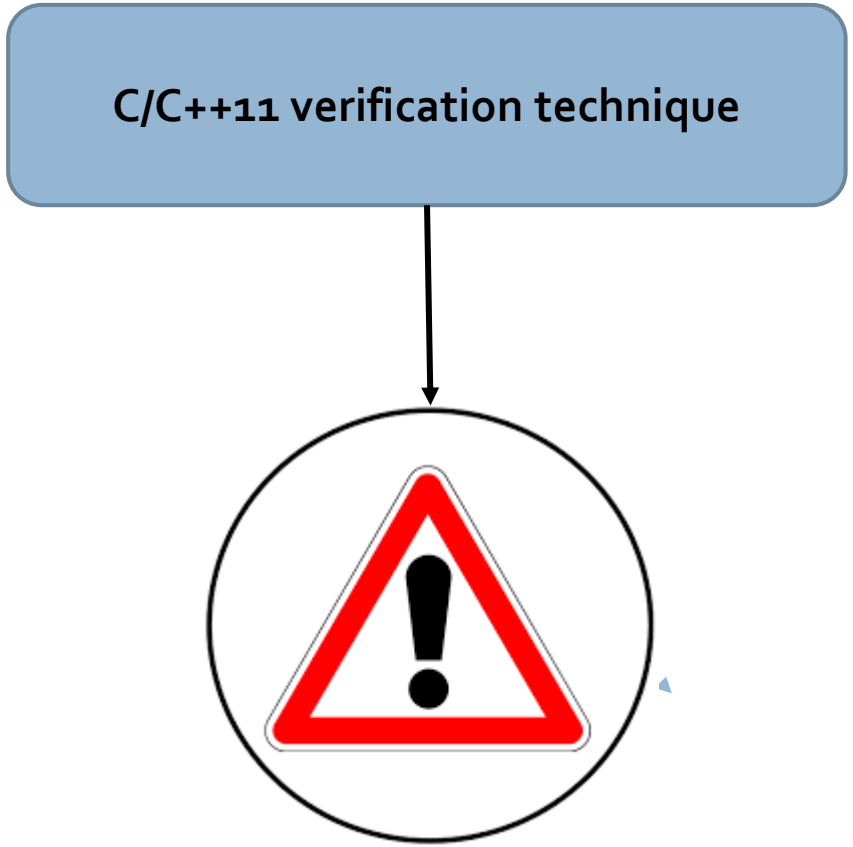


safety property violation

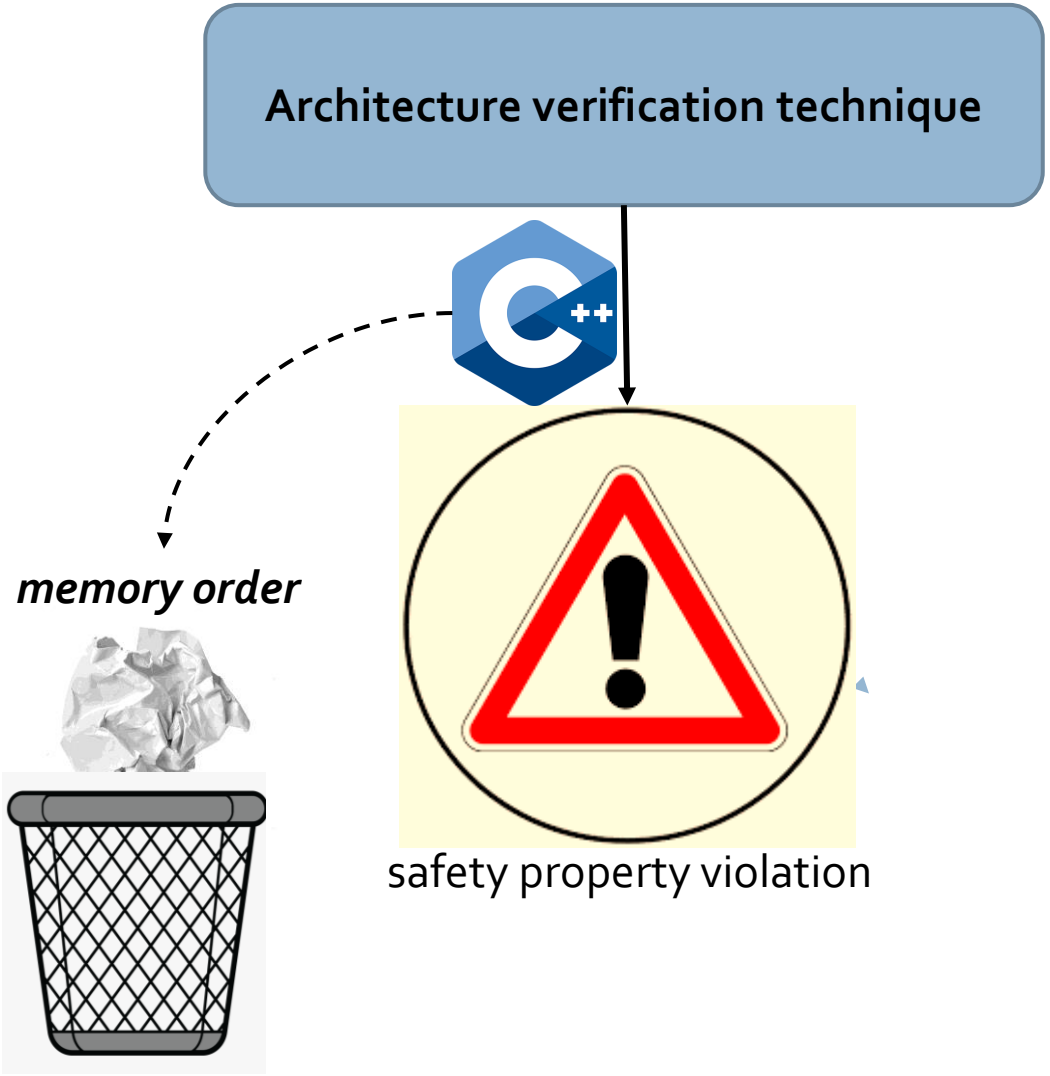
C11 over MCA -- *why?*

C/C++11 verification technique

safety property violation

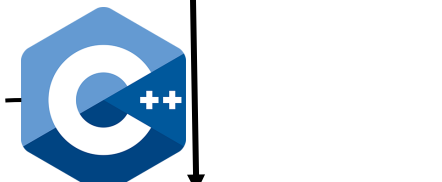
false positive?

C11 over MCA -- *why?*

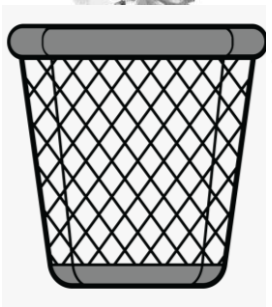


C11 over MCA -- *why?*

Architecture verification technique



memory order



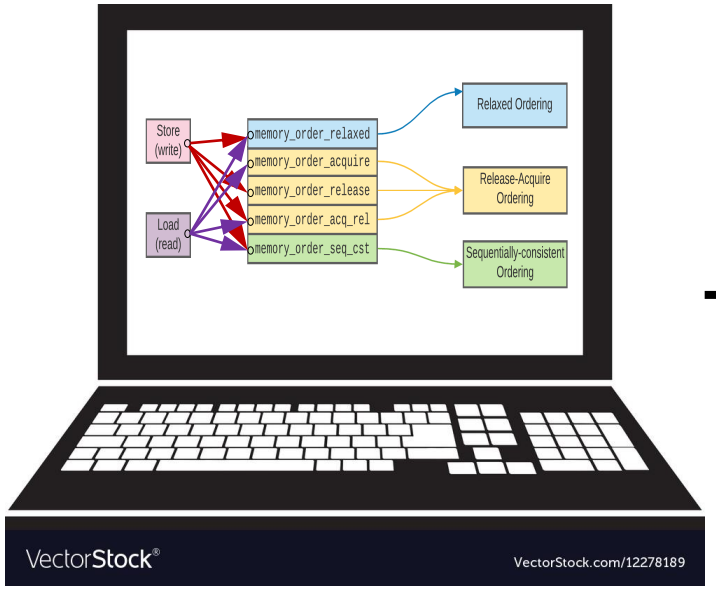
safety property violation

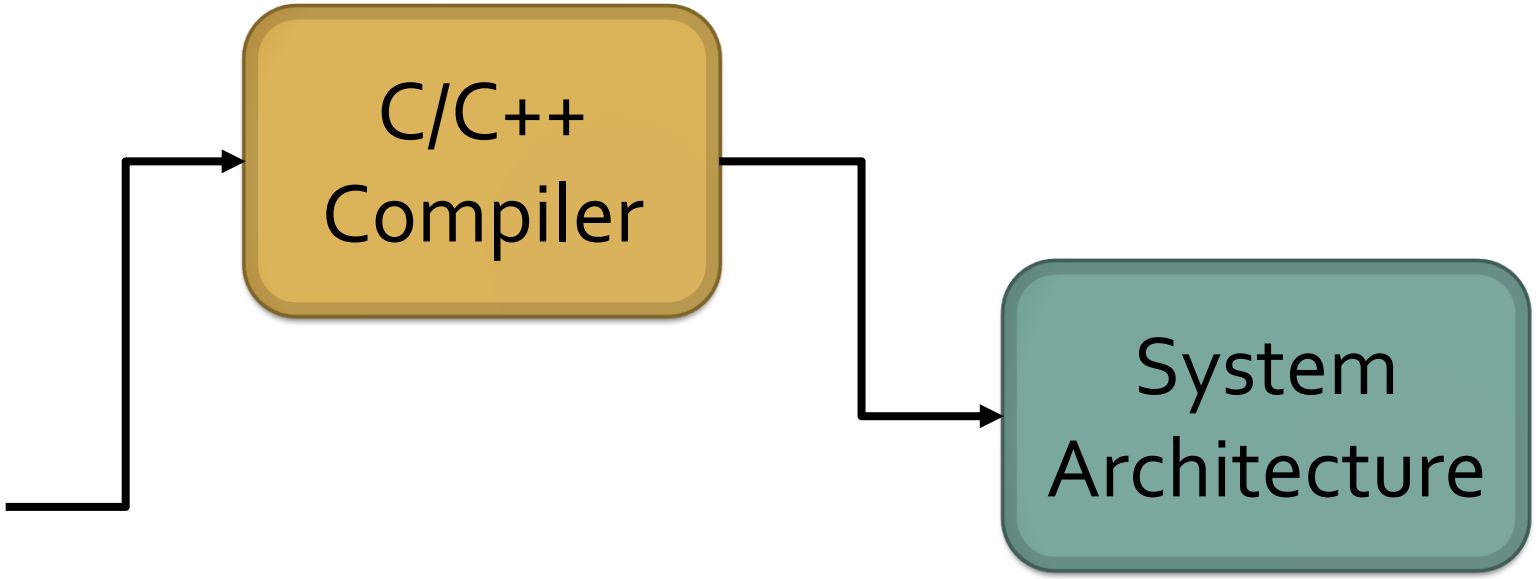
false positive?

false negative?

C11 over MCA -- *why?*

Given a reordering specification





What behaviors can manifest on the underlying architecture?

C11 over MCA -- *why?*

Architecture verification technique

C/C++11 verification technique

false negative?
false positive?

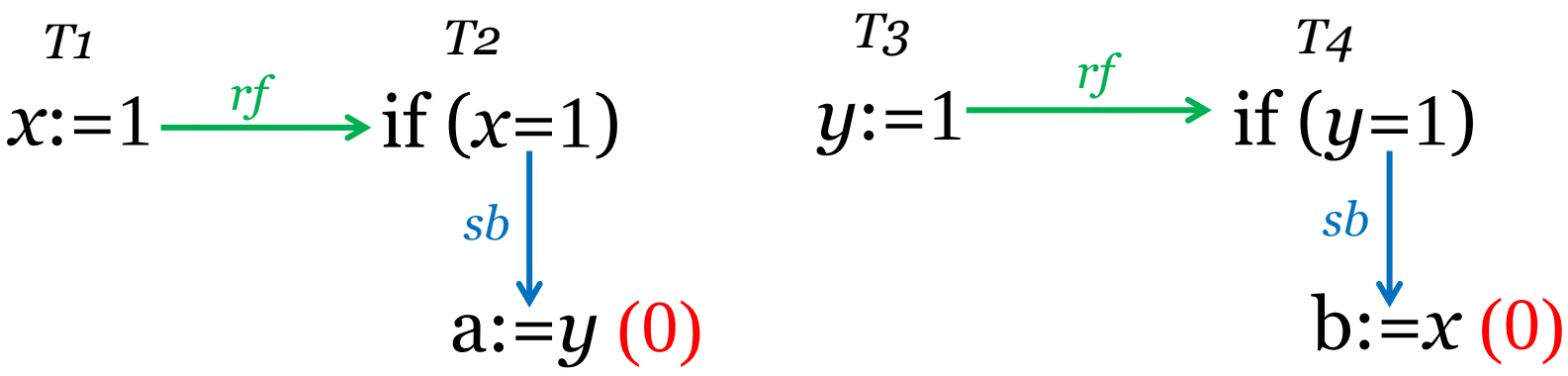
safety property violation

safety property violation

false positive?

C11 over MCA

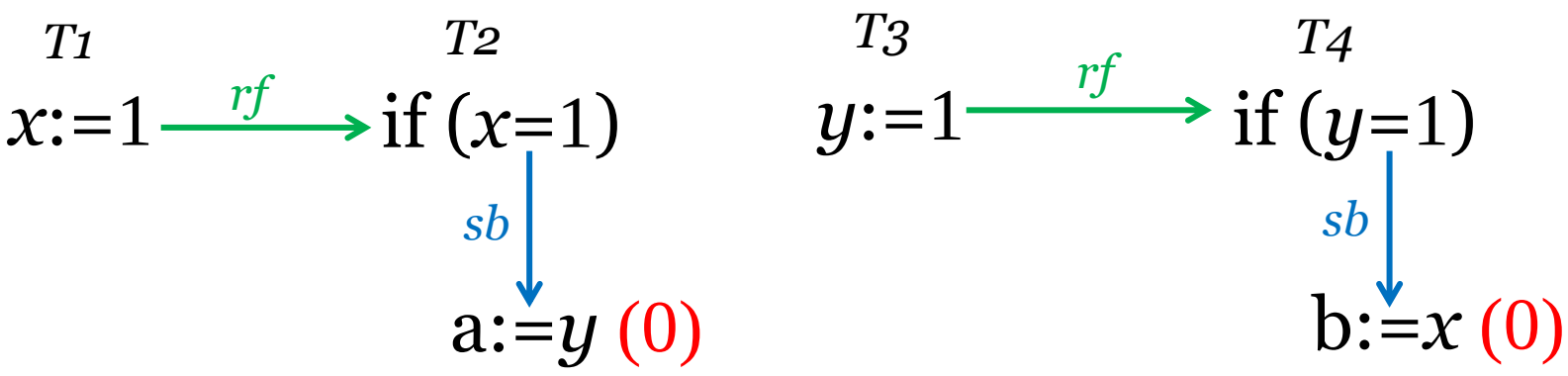
(IRIW) allowed under C11



TASK: Modify event relations to restrict C11 behaviors to MCA memory model

C11 over MCA

(IRIW) allowed under C/C++11



TASK: Modify event relations to restrict C11 behaviors to MCA memory model

[Colvin and Smith, FM 2018].

TASK: Modify event relations and rules to restrict C11 behaviors to MCA memory model

PART I: Define an appropriate happens-before relation

PART II: Define appropriate coherence rules to ensure coherence *wrt* C11

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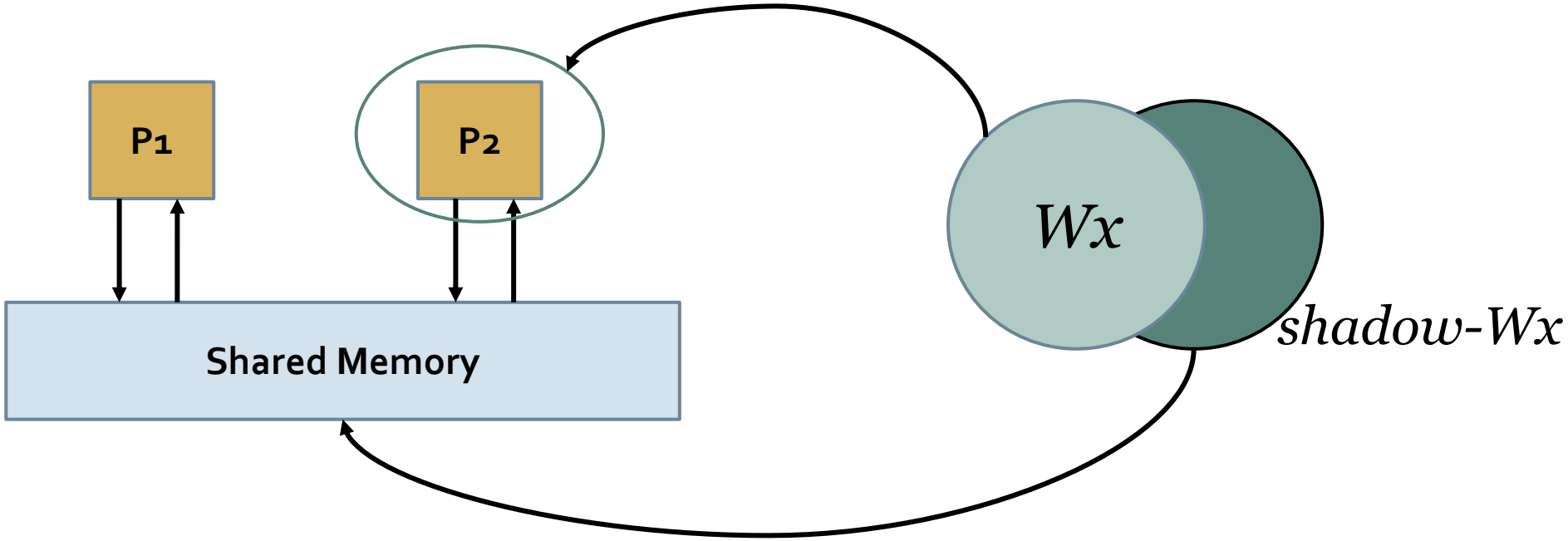
through interleaving

Reordering *through* Interleaving



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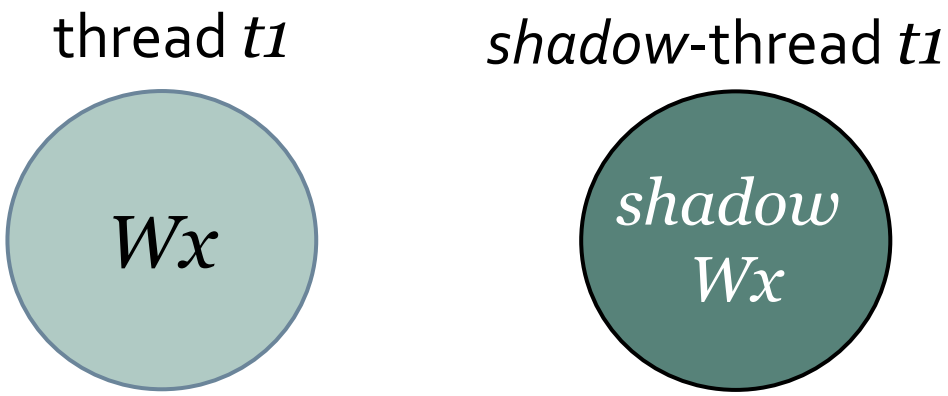

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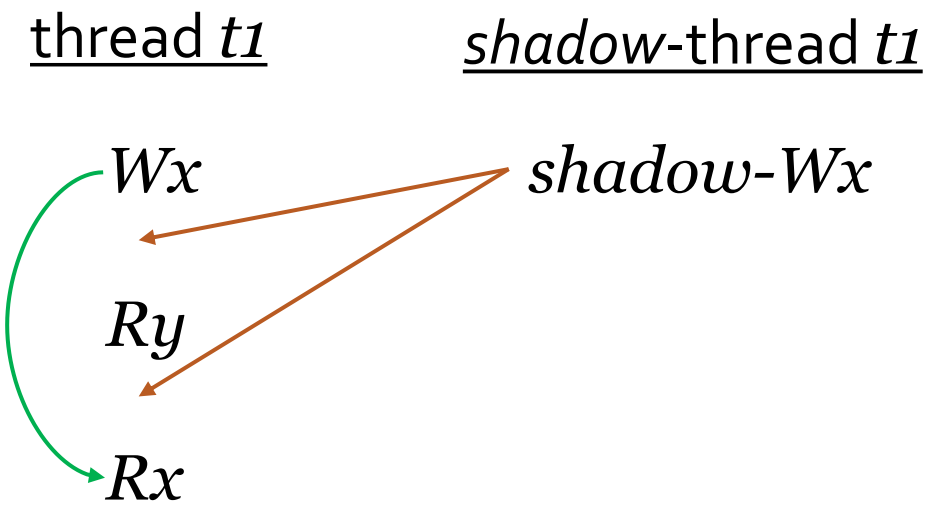
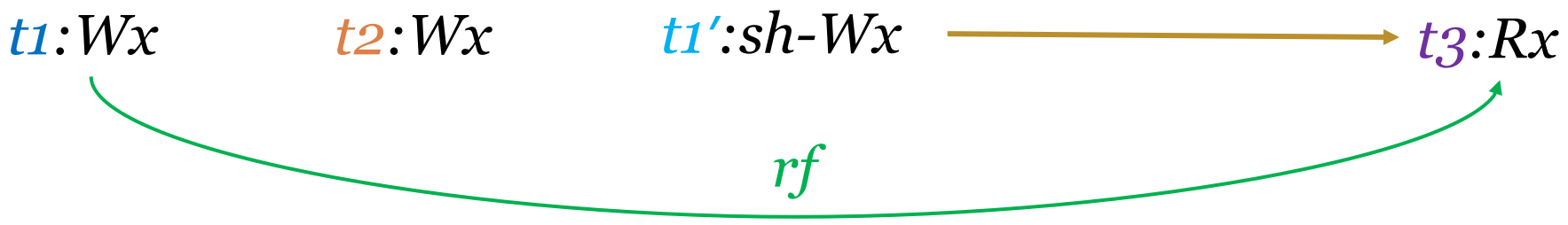


C11 over MCA: axiomatic definition

reads-from (*rf*)



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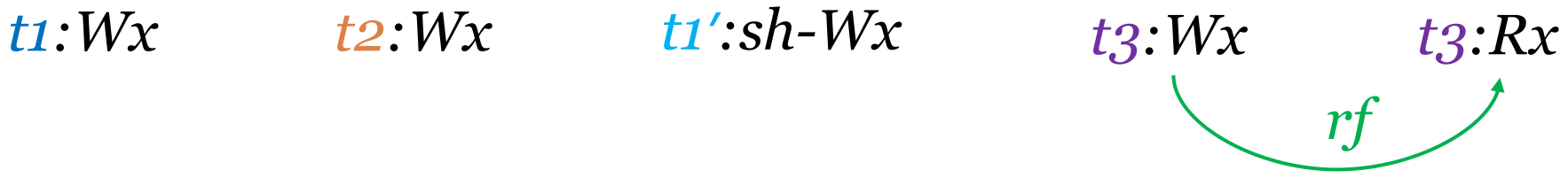

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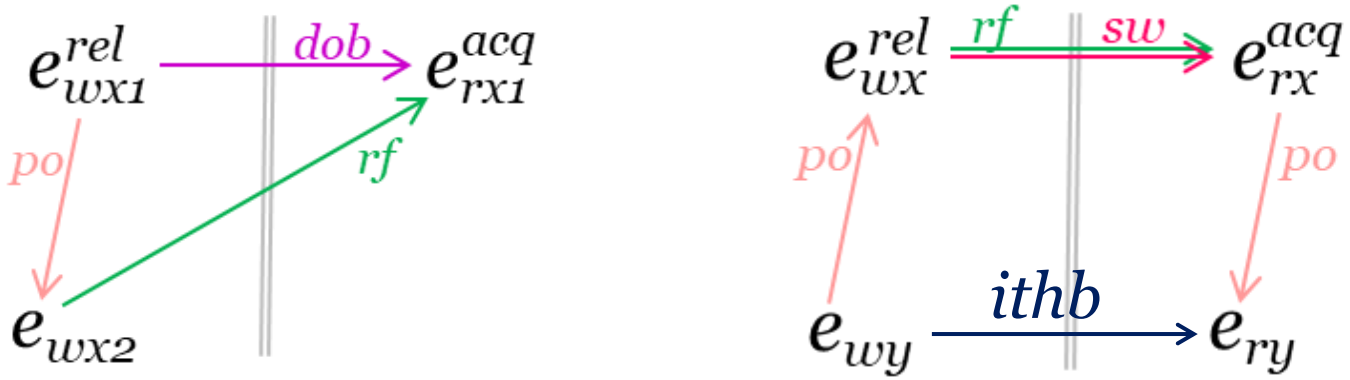
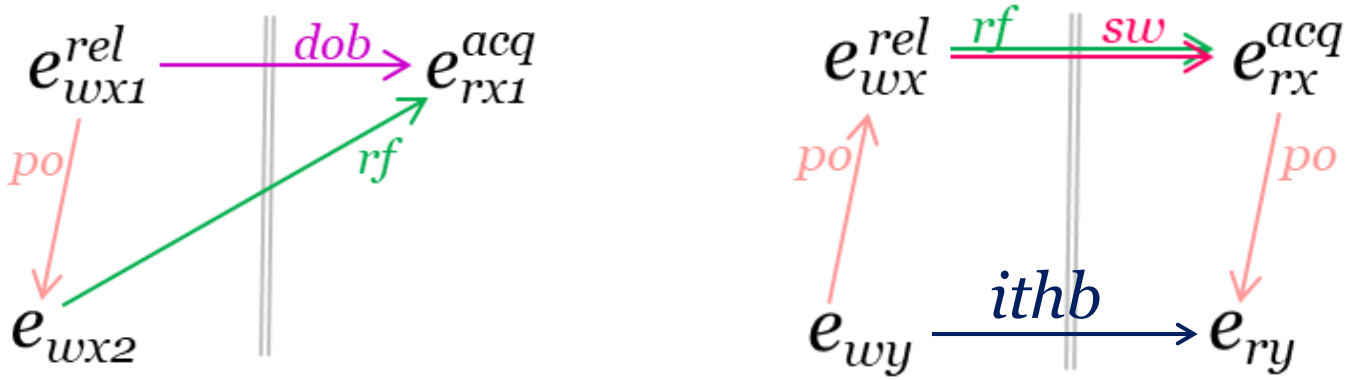


$$e' \rightarrow^{\mathbf{hb}}_{\tau} e \text{ if}(e' \rightarrow^{\mathbf{po}}_{\tau} e \vee e' \rightarrow^{\mathbf{sw}}_{\tau} e \vee e' \rightarrow^{\mathbf{dob}}_{\tau} e\ )^{+}$$

C11 over MCA: axiomatic definition

Theorem 1. $\rightarrow_{\tau}^{hb}$ *for any sequence* τ *is* <u>*valid*</u>

[Abdulla et al., POPL 2014]



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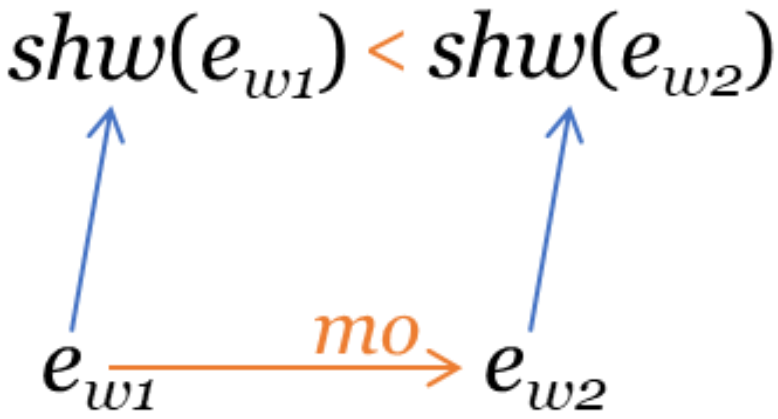

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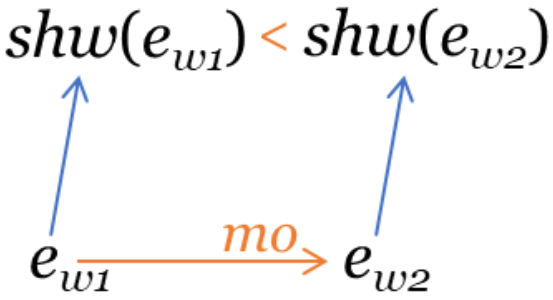

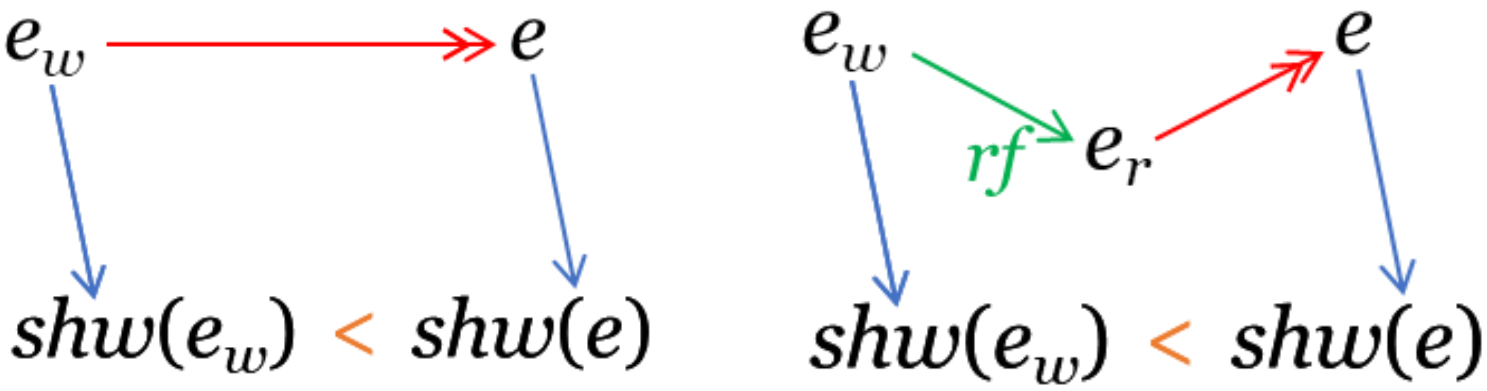

(shmo1)

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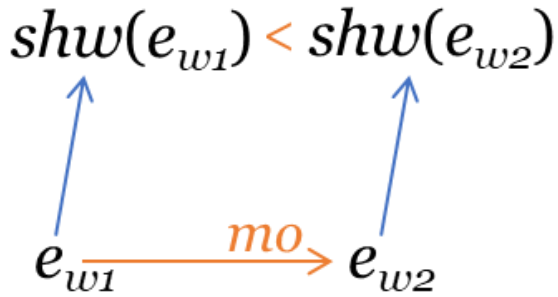

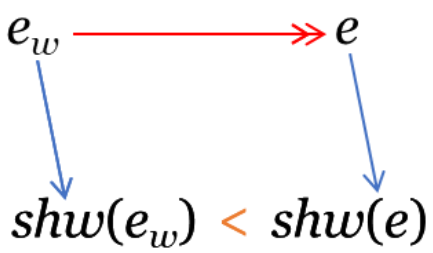

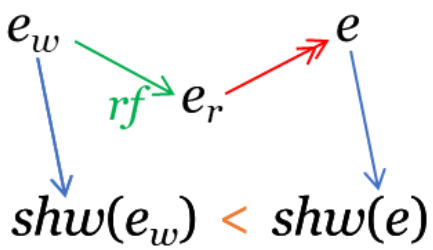

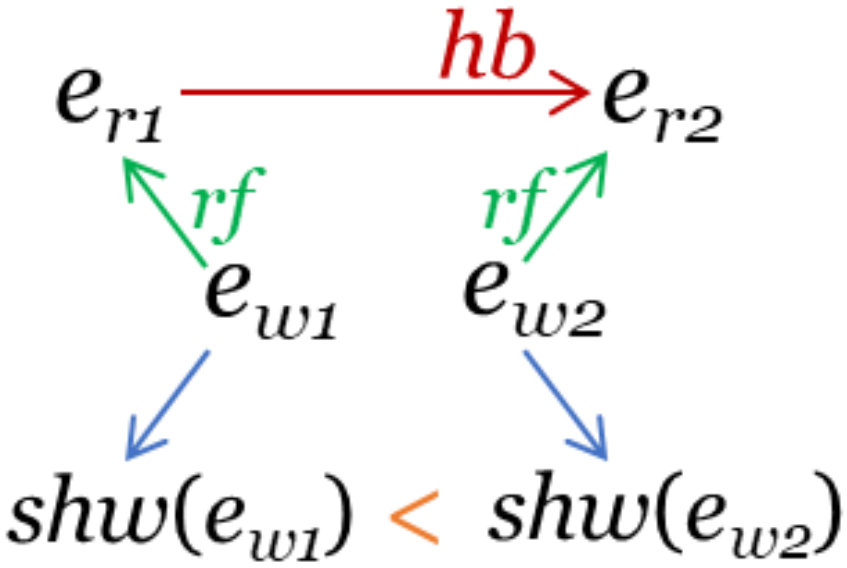

(shmo2)

C11 over MCA: axiomatic definition

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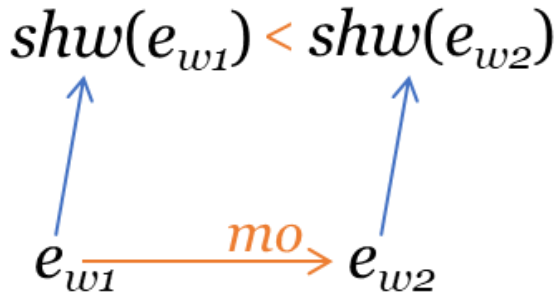
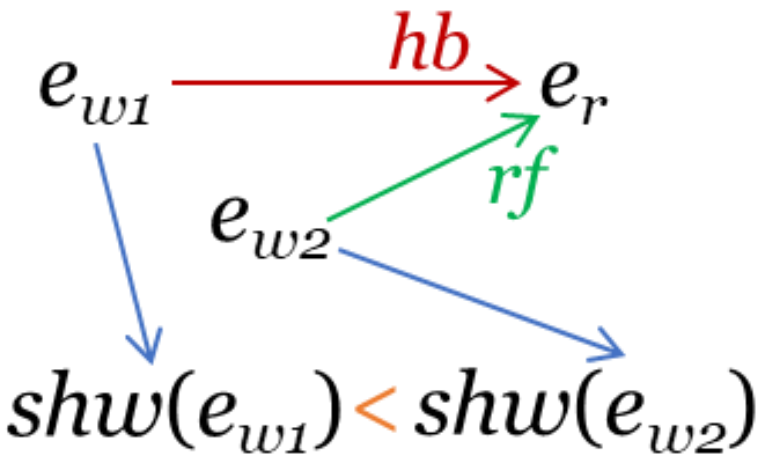
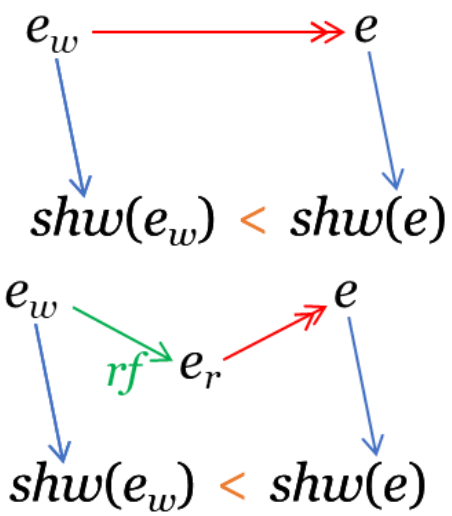
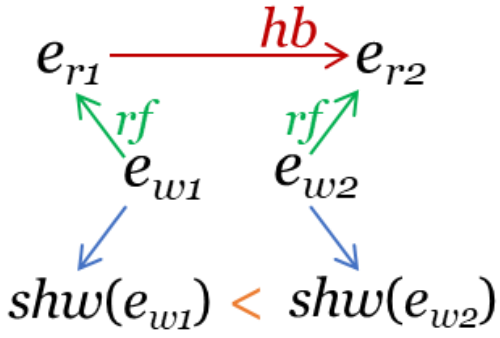




(shmo3)





C11 over MCA: axiomatic definition

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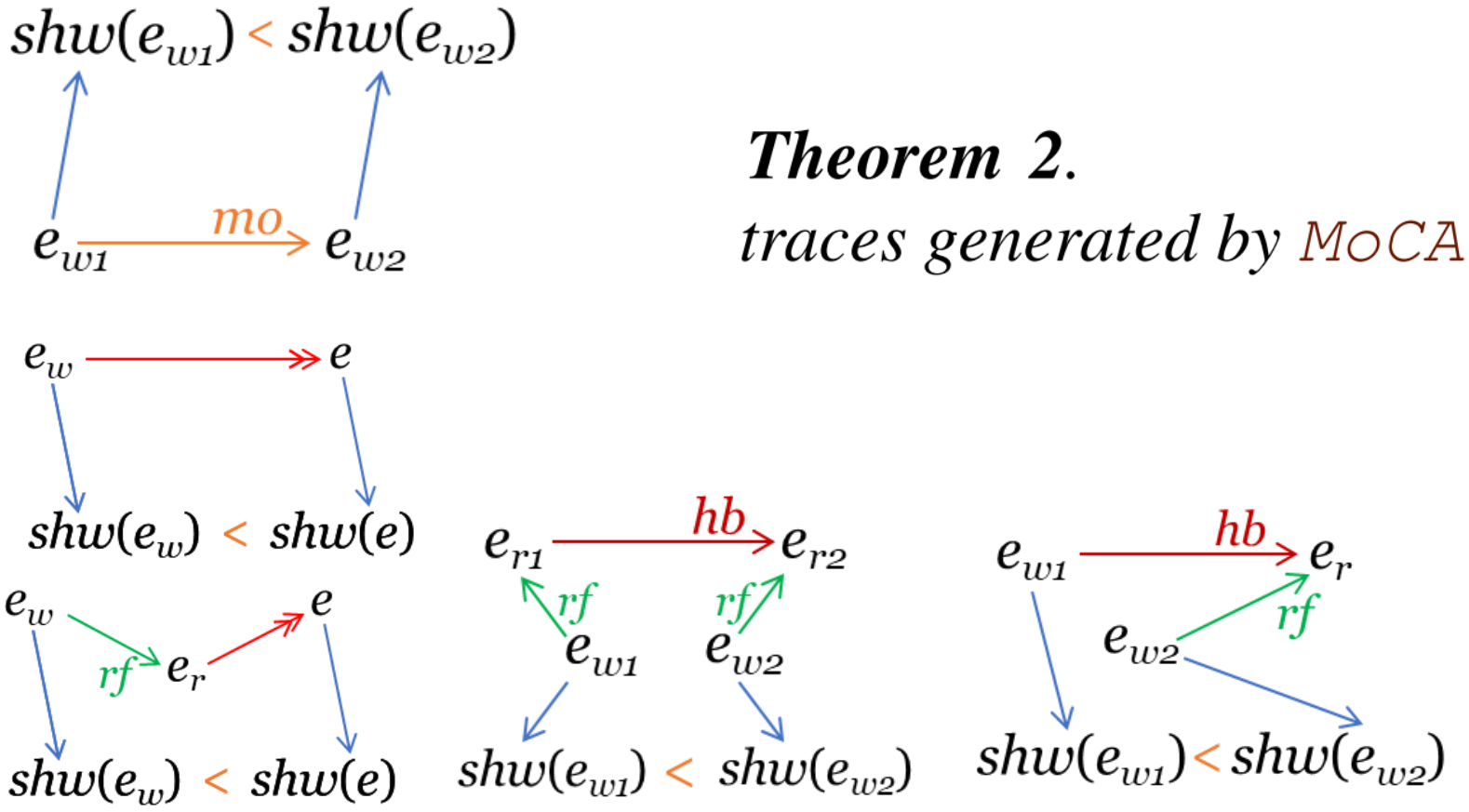
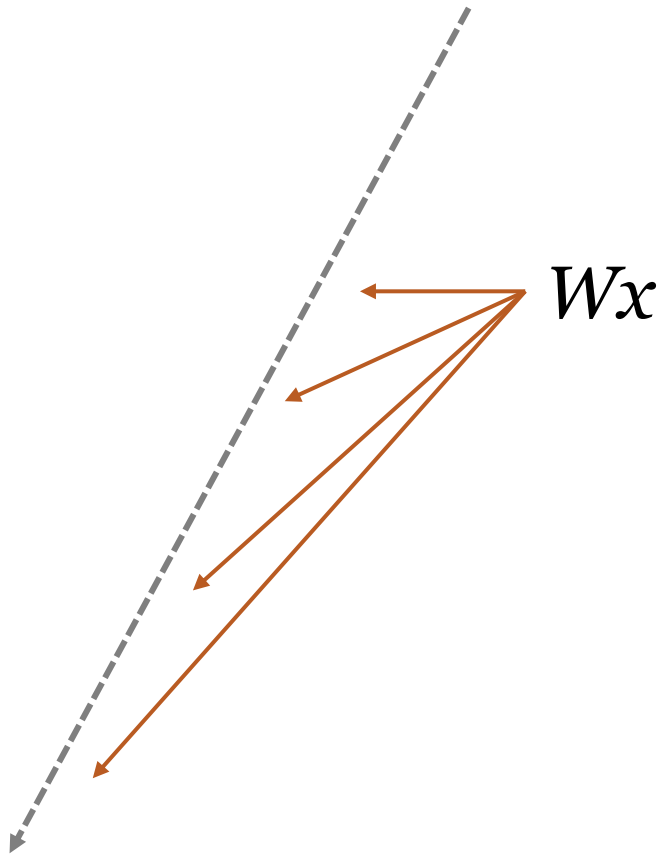


Theorem 2.
traces generated by MoCA *are coherent under C11*

Reordering *through* Interleaving



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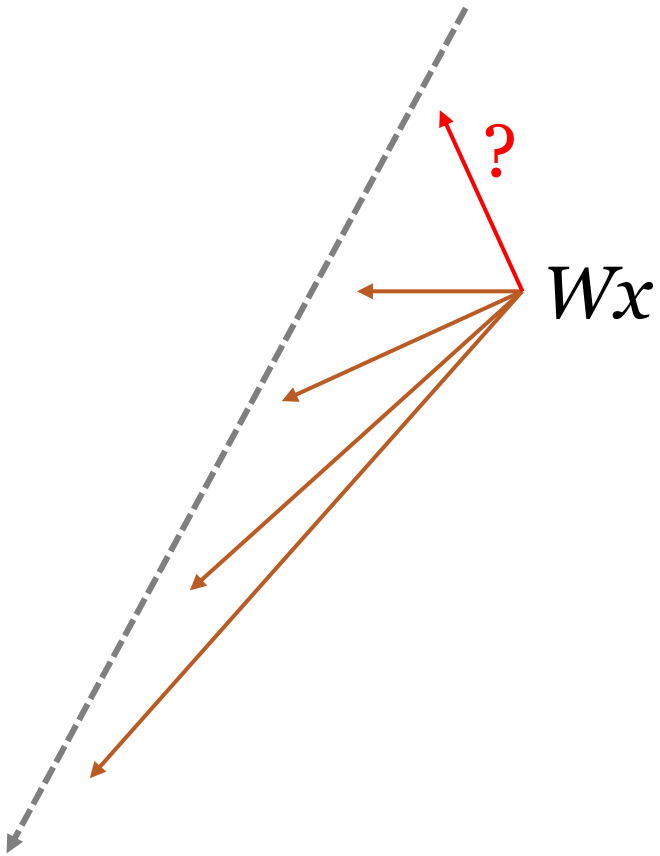
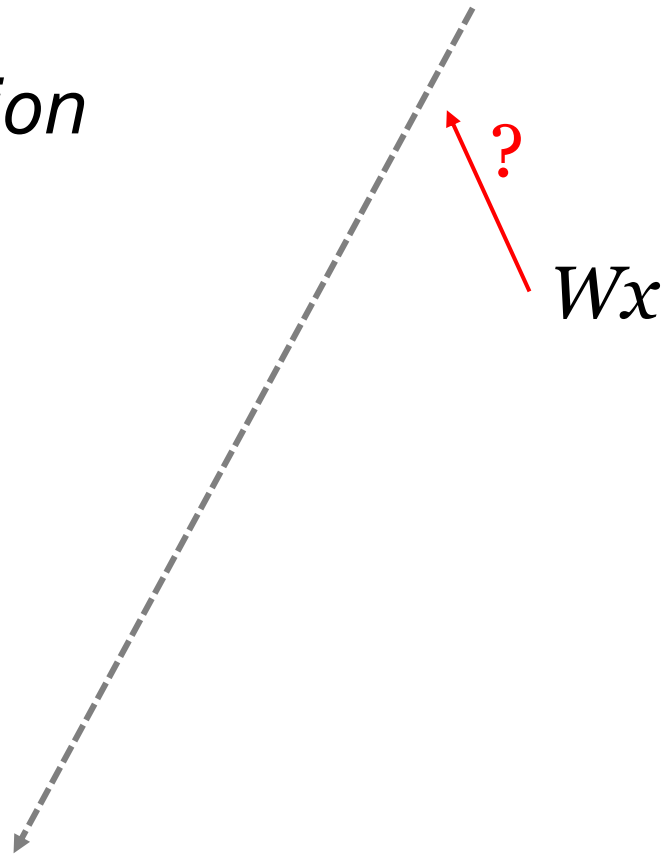


Reordering *through* Interleaving

Early-write Transformation



Reordering *through* Interleaving

Early-write Transformation

<u>thread *ti*</u>

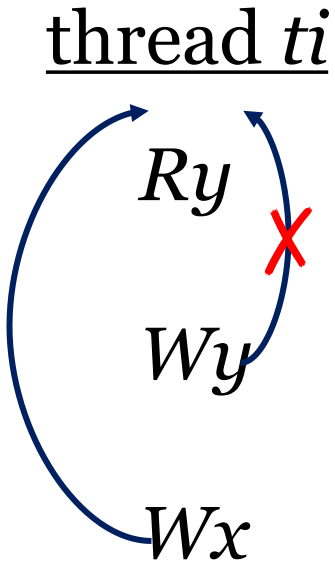
Ry

Wy

Wx

Reordering *through* Interleaving

Early-write Transformation



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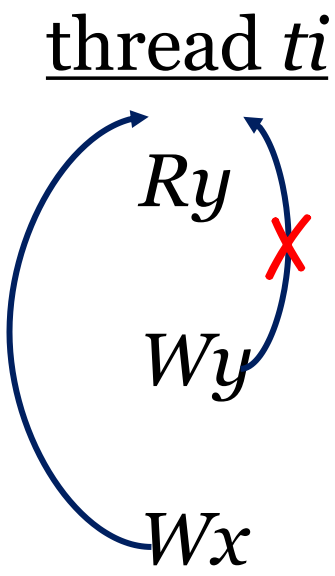
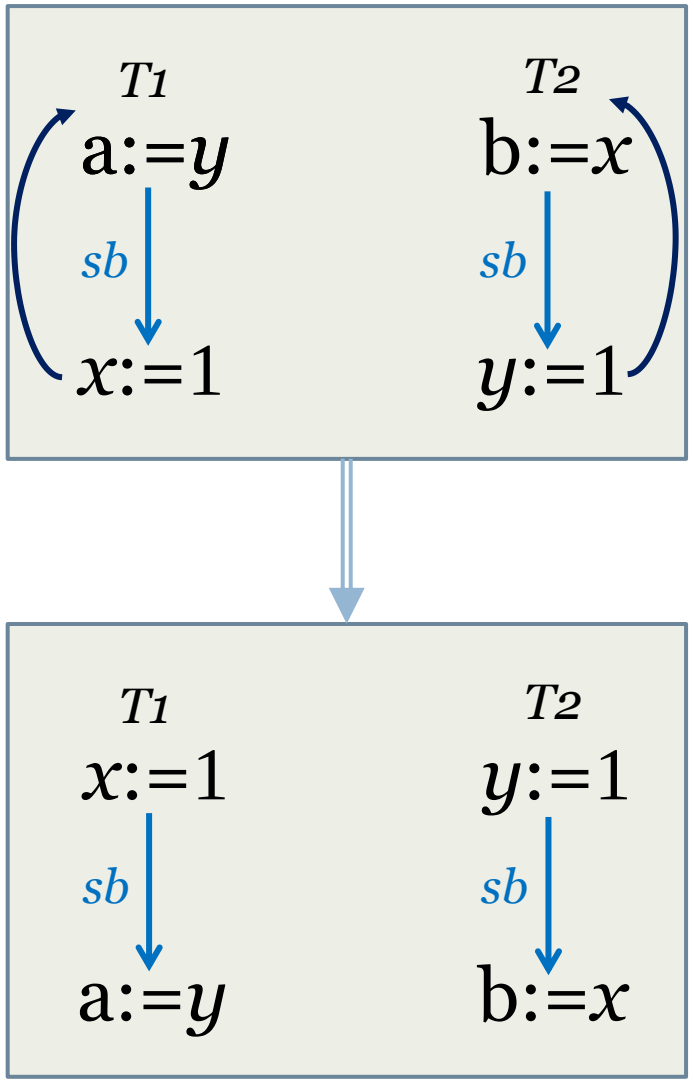


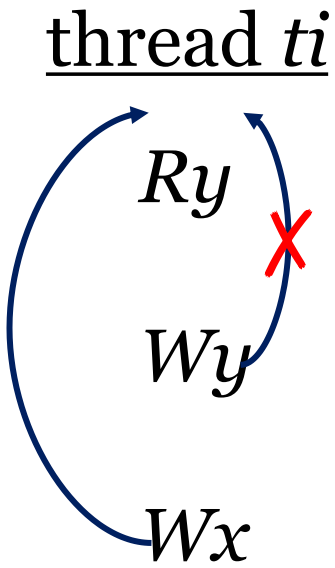


Reordering *through* Interleaving

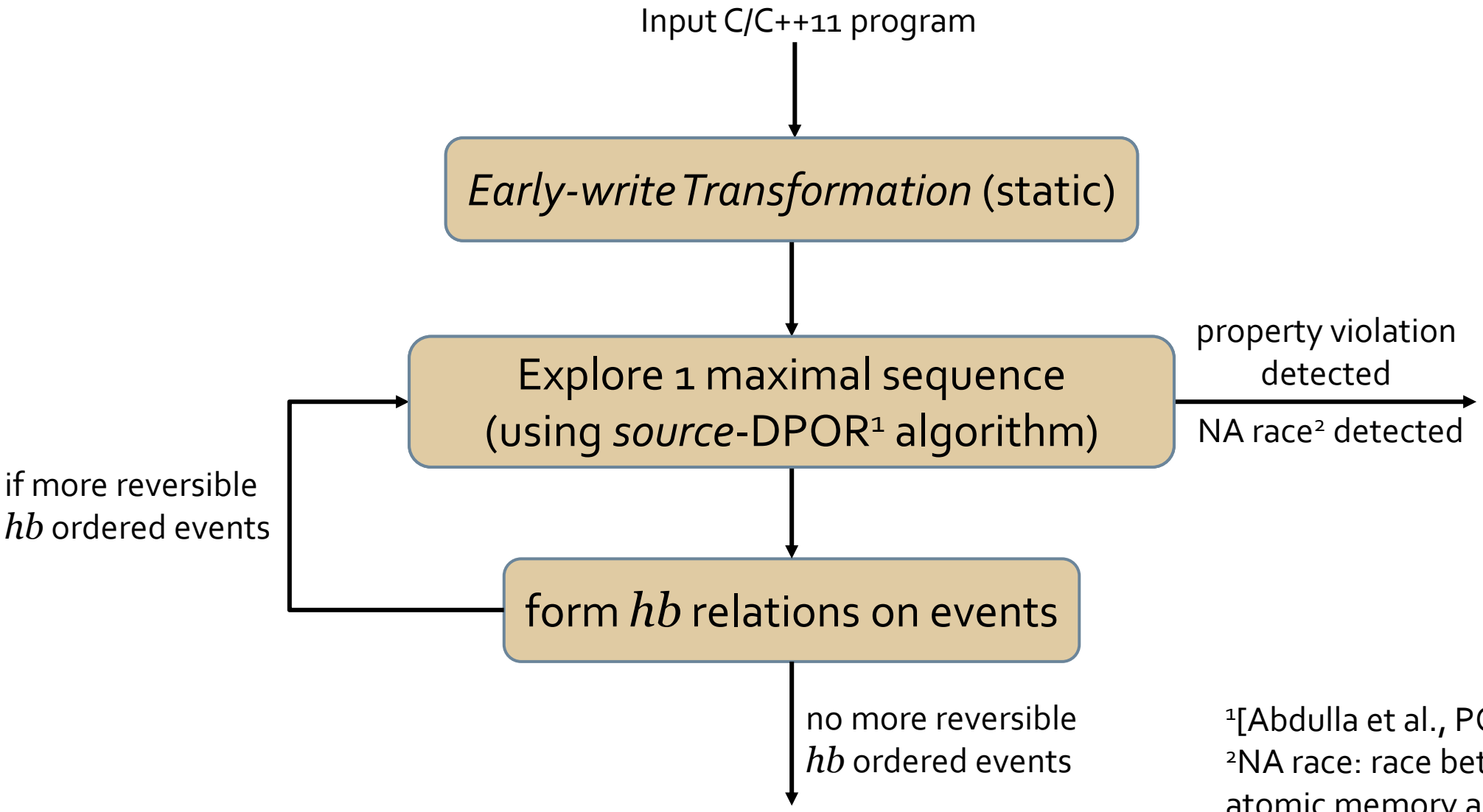
Early-write Transformation

Theorem 3. *Early-write (P to $\widehat{P}$) is semantic preserving.*

MCA model [Colvin and Smith, FM 2018]



MOCA's Technique

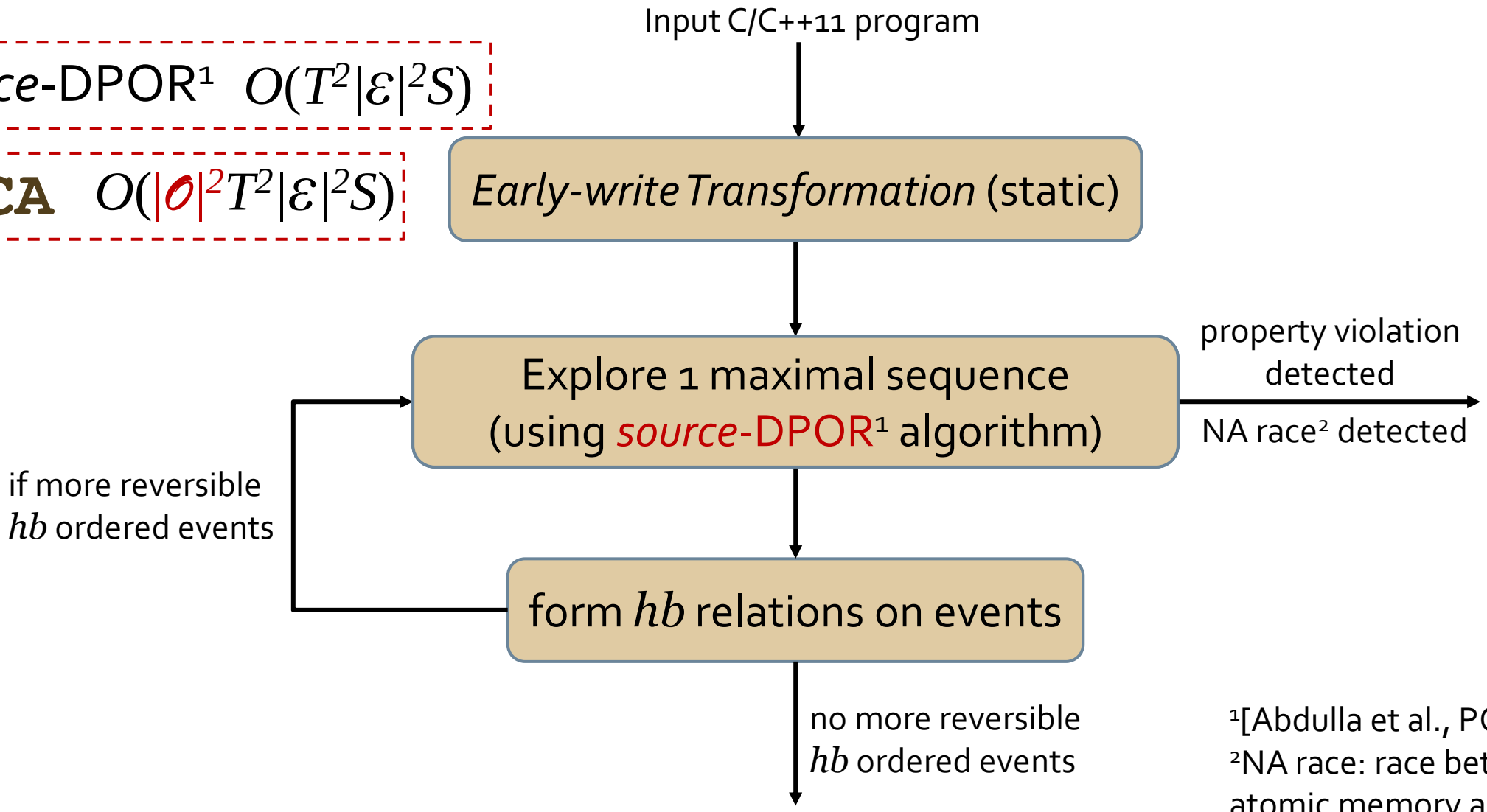


[1][Abdulla et al., POPL 2014]
[2]NA race: race between non-atomic memory accesses

MOCA's Technique

source-DPOR[1] $O(T^2|\mathcal{E}|^2S)$

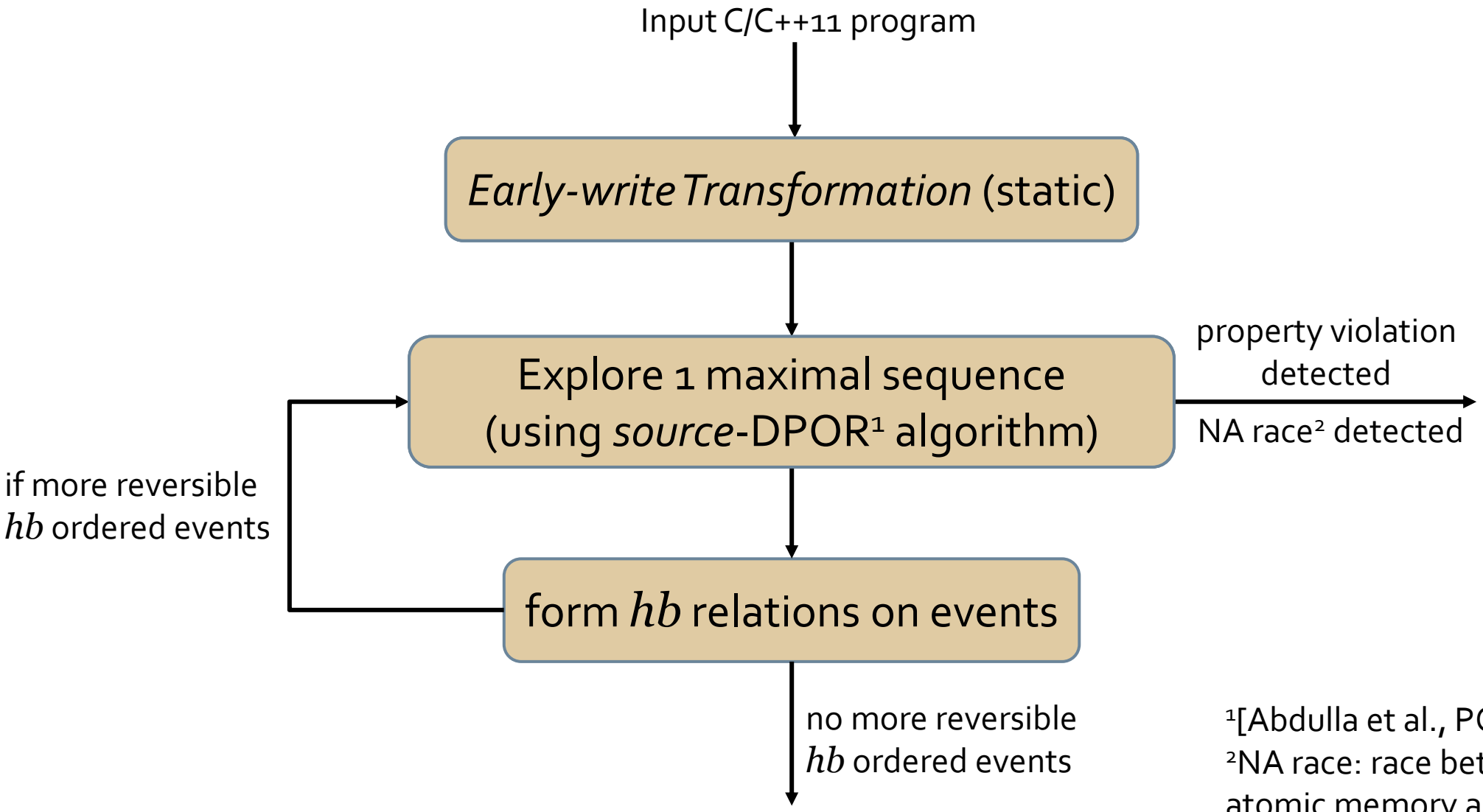
MOCA $O(|\mathcal{O}|^2T^2|\mathcal{E}|^2S)$



[1][Abdulla et al., POPL 2014]
[2]NA race: race between non-atomic memory accesses

MOCA's Technique

Theorem 4. *MoCA traces are equivalent to C11 traces valid over MCA*



[1][Abdulla et al., POPL 2014]
[2]NA race: race between non-atomic memory accesses

Comparative Results on litmus tests

Test	MoCA			CDSChecker			GenMC			HMC		
	M	N	Time	M	N	Time	M	N	Time	M	N	Time
WRC+addrs(7)	7	0	0.03s	7	1	0.01s	7	1	0.02s	7	1	0.03s
WR-ctrl(4)	7	0	0.03s	4	2	0.01s	4	2	0.02s	4	2	0.02s
Z6+poxxs(4)	18	0	0.12s	14	4	0.01s	4	4	0.03s	4	4	0.03s
IRIW+addrs(15)	15	0	0.07s	15	1	0.01s	15	1	0.02s	15	1	0.02s
WW+RR(15)	96	0	0.53s	15	66	0.02s	15	66	0.02s	15	66	0.02s

M: #*MCA* sequences, N: #non-*MCA* sequences

CDSChecker [Norris and Demsky, OOPSLA 2013]
GenMC [Kokologiannakis et al., POPL 2017]
HMC [Kokologiannakis and Vafeiadis , ASPLOS 2020]

Comparative Results on litmus tests

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	M	N	Time	M	N	Time	M	N	Time	M	N	Time
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IRIW+addrs(15)	15	0	0.07s	15	1	0.01s	15	1	0.02s	15	1	0.02s
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M: #*MCA* sequences, N: #non-*MCA* sequences

CDSChecker [Norris and Demsky, OOPSLA 2013]
GenMC [Kokologiannakis et al., POPL 2017]
HMC [Kokologiannakis and Vafeiadis , ASPLOS 2020]

Comparative Results on benchmarks

Test	MoCA		CDSChecker		GenMC		HMC	
	#Seq	Time	#Seq	Time	#Seq	Time	#Seq	Time
mutex	5	0.02s	2-NVs	0.01s	NV	0.03s	NV	0.02s
peterson	13	0.15s	666-NVs	2.73s	NV	0.02s	NV	0.02s
RW-lock	246	0.52s	193-NVs	0.38s	NV	0.02s	NV	0.04s
spinlock	506	16.98s	TO	-	NV	0.08s	NV	0.15s
fibonacci-2	667	5.57s	TO	-	NV	0.04s	NV	0.03s
fibonacci-3	10628	2m14s	TO	-	NV	0.06s	NV	0.07s
fibonacci-4	92421	56m21s	TO	-	NV	0.13s	NV	0.31s
counter-5	3599	39.78s	25-NVs	0.31s	NV	0.06s	NV	0.03s
counter-10	55927	12m53s	100-NVs	9.21s	NV	0.05s	NV	0.07s
counter-15	TO	-	225-NVs	50.31s	NV	0.11s	NV	0.16s
flipper-5	2489	20.19s	201-NVs	3.26s	NV	0.03s	NV	0.04s
flipper-10	96737	6m12s	TO	-	NV	0.04s	NV	0.02s
flipper-15	TO	-	TO	-	NV	0.03s	NV	0.03s
prod-cons-10	9373	1m23s	TO	-	NV	0.04s	NV	0.04s
prod-cons-15	38593	6m46s	TO	-	NV	0.02s	NV	0.02s
prod-cons-20	109838	20m28s	TO	-	NV	0.02s	NV	0.02s

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prod-cons-15	38593	6m46s	TO	-	NV		NV	
prod-cons-20	109838	20m28s	TO	-	NV		NV	

Thank You

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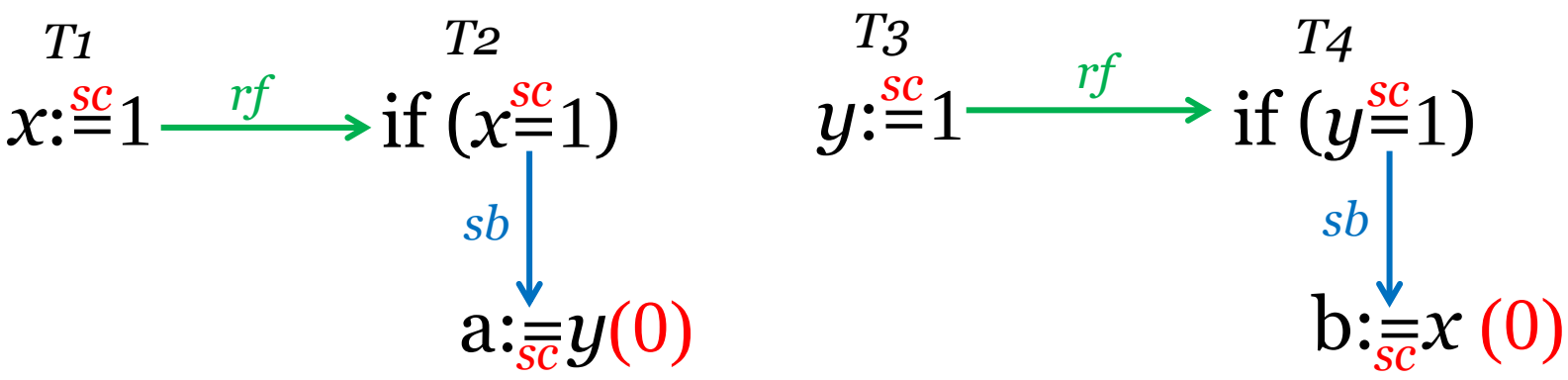
C/C++11 over MCA

(IRIW) allowed under C/C++11 *unless all events are sc ordered*



specified as:

```
x.store(1, memory_order_seq_cst);
x.load(memory_order_seq_cst);
```

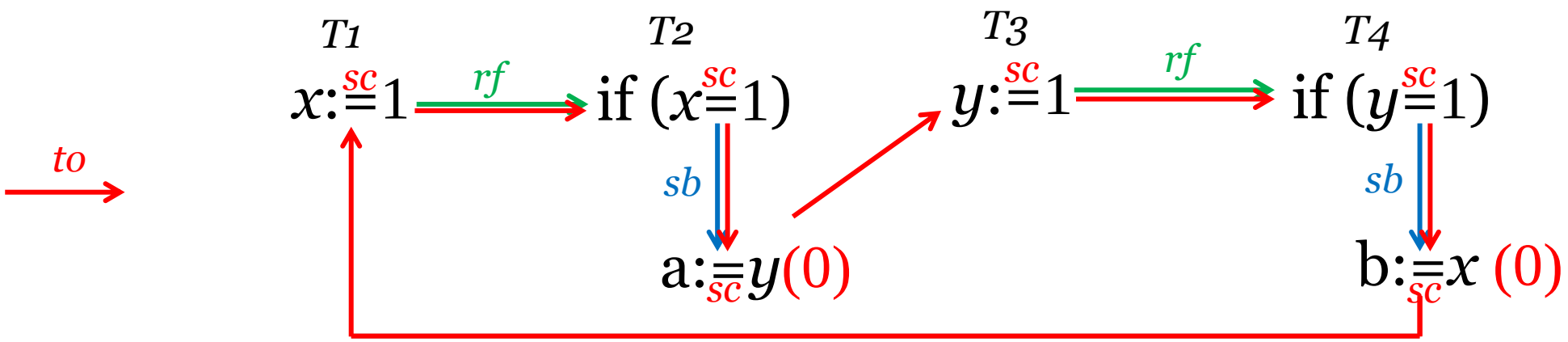
other memory orders:

rlx ⊏ {*rel*, *acq*} ⊏ *acq-rel* ⊏ *sc*

back

C/C++11 over MCA

(IRIW) allowed under C/C++11 *unless all events are sc ordered*



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other memory orders:

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back

SUB-TASK: Identify MCA model semantics [Colvin and Smith, FM 2018]

Due to the ***dynamic*** nature of technique

- ~~local operations~~
- ~~branches and paths~~

$$\frac{c \xrightarrow{\beta} c' \quad \alpha \overset{\mathrm{R}}{\Leftarrow} \beta_{[\alpha]}}{(\alpha\,;\ c) \xrightarrow{\beta_{[\alpha]}} (\alpha\,;\ c')}$$

(reordering)

$$\frac{c \xrightarrow{x\,:=\,r} c' \quad \sigma(r) = v}{(\mathbf{lcl}\ \sigma \bullet c) \xrightarrow{x\,:=\,v} (\mathbf{lcl}\ \sigma \bullet c')}$$

(write-issue)

$$\frac{c \xrightarrow{r\,:=\,x} c'}{(\mathbf{lcl}\ \sigma \bullet c) \xrightarrow{[x=v]} (\mathbf{lcl}\ \sigma_{[r\,:=\,v]} \bullet c')}$$

(read-shared)

$$\frac{p \xrightarrow{\mathrm{N}:x\,:=\,e} p'}{(\mathbf{glb}\ \sigma \bullet p) \xrightarrow{\tau} (\mathbf{glb}\ \sigma_{[x\,:=\,e_\sigma]} \bullet p')}$$

(write-update)

$$\frac{p_1 \xrightarrow{\alpha} p_1'}{p_1 \parallel p_2 \xrightarrow{\alpha} p_1' \parallel p_2} \qquad \frac{p_2 \xrightarrow{\alpha} p_2'}{p_1 \parallel p_2 \xrightarrow{\alpha} p_1 \parallel p_2'}$$

(parallel-composition)

back